STUDY OF III-N HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

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STUDY OF III-N HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

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SUMMARY

This thesis describes the design, fabrication and characterization of AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) grown by a Metal Organic Chemical Vapor Deposition (MOCVD) on sapphire substrates. The objective of this research is to develop AlGaN/GaN power devices with high breakdown voltage (greater than 1 kV) and low turn-on resistance. Various characteristics such as current drive (I_{dss}), transconductance (g_m) and threshold voltage (V_{th}) have also been measured and the results have been discussed. Two major challenges with the development of high breakdown voltage AlGaN/GaN HFETs have been high material defect density and non-optimized fabrication technologies which gives rise to buffer leakage and surface leakage, respectively. In this thesis, mesa isolation, ohmic and gate metal contacts, and passivation techniques, have been developed to improve the performance of these power transistors in terms of low contact resistance and low gate leakage. The relationship between breakdown voltage and $R_{ds(ON)}A$ with respect to the gate-drain length *(L_{gd})* is also discussed. First, unit cell devices were designed (two-fingered cells with W_g = 100, 300, 400 μm) and characterized, and then they were extended to form large area devices (up to W_g = 40 mm). The design goals were classified into three parts:

- **High breakdown voltage**: This was achieved by designing devices with variations in L_{gd},
- **Low turn-on resistance**: This was achieved by studying the annealing temperatures, incorporating additional thick metal pads, as well as studying the passivation etch recipe in terms of various parameters such as the ratios of CF_4 and Ar, etch rate, etch time, etc., as un-optimized etching recipe can increase

the turn-on resistance,

- **Low gate leakage**: The gate leakage was reduced significantly by using a gate metal with a larger barrier height after a series of experiments, optimizing the deposition rate for the metal, and optimizing the thickness of the metal for improved device performance.

All devices with L_{gd} larger than 10 μm exhibited excellent breakdown voltage characteristics of over 800 V, and it progressed as the L_{gd} increased. The turn-on resistance was also reduced significantly below 20 mΩ-cm^2, for devices with L_{gd} = 15, 25, and 20 μm. The gate leakage was measured for all devices to 200 V, and was in the range of 10-100 nA, which is one of the best values reported for multi-fingered devices with L_{gd} in the range of 2.4 to 5 mm. Some of the key challenges faced in fabrication were determining a better gate metal layer to reduce gate leakage, optimizing the passivation via etch recipe, and reducing surface leakage.

The thesis is divided into the following sections: Chapter 1 provides an introduction to III-N semiconductors and HFETs; Chapter 2 provides a background on the theory of III-N semiconductors and design considerations used for the devices; Chapter 3 discusses the device processing development by providing an overview on the layer structures, layout design, device fabrication, and characterization; Chapter 4 discusses the results obtained; and Chapter 5 concludes the study along with scope for improvement and future work.

CHAPTER I

INTRODUCTION

Technological advances in recent decades have shown that the use of Silicon (Si) has approached its theoretical limits. It is observed that the performance of Si degrades at high temperatures and high power. Devices that can be operated at high power and high temperatures require high breakdown voltages, high thermal conductivities and high switching speeds, in addition to manufacturability and low cost [1]. Therefore, electronic systems that demand high-temperatures and high power are now being realized using wide bandgap semiconductors like Silicon Carbide (SiC) or Gallium Nitride (GaN), due to their superior electrical properties, such as large and direct band gap. For III-N materials, the bandgap varies from 0.6 eV for InN through 3.4 eV for GaN to 6.2 eV for AlN, and is illustrated in Figure 1. Due to this wide range of bandgaps available, III-N materials are used for a myriad of applications ranging from LEDs to high power and high frequency applications.

Since the early 1990s, Galium Nitride (GaN) has shown interesting and very promising characteristics for optoelectronic and high power applications . Over the last two decades, a significant amount of research has been done to enhance the properties of these devices in terms of material quality as well as fabrication techniques. GaN-based optical applications have reached the stage of commericalization, while high power and microwave electronics show a very promising future.

1.1 History and Advancements of GaN HFETs

Some of the key issues that need to be addressed when chosing a semiconductor technology are its:

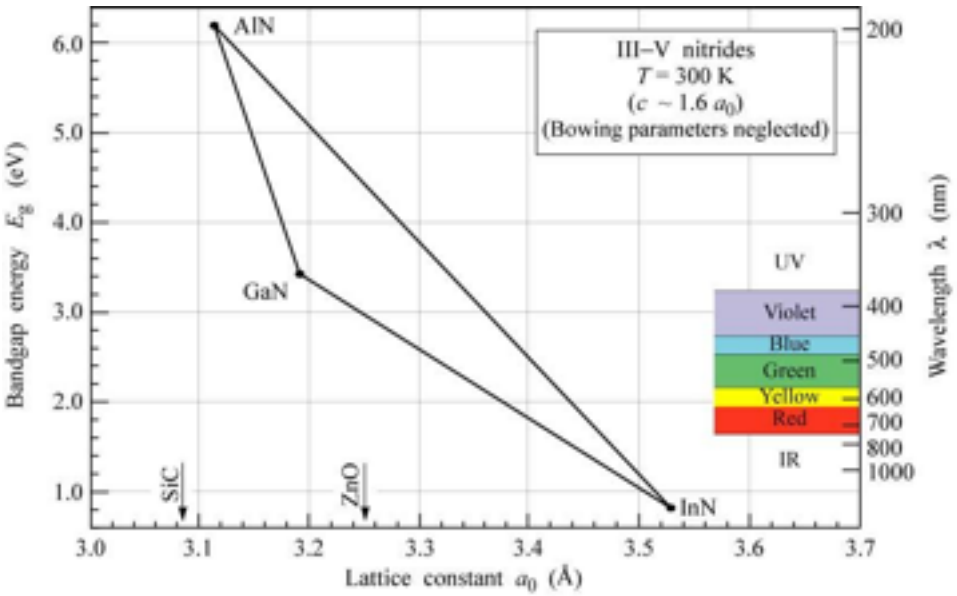


Figure 1: Bandgaps versus lattice constants of important semiconductors at room temperature [23].

- Advantages and disadvantages over existing material systems
- Application areas
- Cost and market-value

This section addresses the above points by giving an overview of III-N semiconductors.

Column III of the periodic table consists of elements such as gallium (Ga), aluminum (Al), and indium (In), and these elements form compounds with nitrogen (N) and are called III-Nitride (III-N) compound semiconductors. Contrary to most III-V semiconductors like GaAs with a Zincblende crystal structure, the major crystalline structure of the III-N semiconductors at low pressure is the Wurtzite structure [2]. Illustrated below in Figure 2 is the wurtzite structure for III-N materials [2]. It is hexagonal in planar direction but tetrahedron in vertical direction.

Some important properties of III-N compound semiconductors are listed in Table 1, and is also compared with other important semiconductors such as Si, Ge, and SiC. A large bandgap energy results in high electric field breakdown, and thus enables

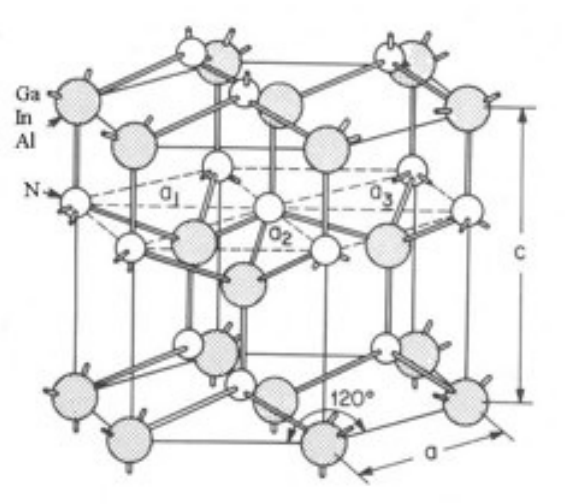


Figure 2: The Wurtzite structure commonly found in the binary III-nitride semiconductors [2].

high-voltage application. Additionally, it also allows the material to withstand high operating temperatures and operation under harsh environments. As can be inferred from the table, GaN and SiC have high bandgap energies, nearly two-three times that of conventional semiconductors.

III-N semiconductors with the wurtzite structure are direct bandgap semiconductors. The bandgap energy of III-N materials can cover the range from 0.7 eV to 6.2 eV. The electric breakdown field is also large in these devices, making them excellent candidates for high power devices. Furthermore, these wide bandgap materials have an advantage over the conventional semiconductors in terms of higher thermal conductivity, and chemical and material stability, making them suitable for high power devices working in harsh environment. With advancement in material growth technologies, the carrier mobility in III-N materials is also much higher than before, making them suitable for high speed devices as well [2].

This thesis is focused on III-N HFET processing development based on AlGaN and GaN heterostructures. GaN was first synthesized by Juza and Hahn in the 1930s by passing ammonia (NH_3) over liquid gallium (Ga) at elevated temperatures [4]. Maruska and Tietjen were the first to try Hydride Vapor Phase Epitaxy (HVPE)

Table 1: Material properties of III-N and conventional semiconductors [28-35].

Material	**GaN**	**AlN**	**InN**	**Si**	**Ge**	**GaAs**	**InP**	**4H-SiC**
Structure	W	W	W	D*	D*	Z	Z	W
Lattice Constant ($\AA$)	a=3.189 c=5.182	a=3.111 c=4.978	a=5.44 c=5.718	5.431	5.646	5.653	5.869	a=3.073 c=10.05
Bandgap (ev)	3.44	6.2	0.7-1.0	1.12	0.66	1.42	1.35	3.26
Nature of Bandgap	D	D	D	I	I	D	D	I
Breakdown Field (MV/cm)	5	1.2-1.8	-	0.25-0.8	0.1	0.3-0.9	0.5	3-5
Electron Saturated Velocity (10^7 cm/s)	2.5	1.9	3.4	2.3	3.1	0.7	3.9	1.9
Electron Mobility (cm^2/V-s)	1000	300	3200	1400	3900	8000	5400	900
Hole Mobility (cm^2/V-s)	400	14	-	500	1900	400	200	120
Thermal Conductivity ($W/cm^{-1}K^{-1}$)	2.0-2.4	3.0-3.3	0.6-1.0	1.56	0.58	0.46	0.68	3.7
Dielectric Constant (static)	10.4	8.5	15.3	11.7	16.0	12.9	12.6	9.66
Refractive Index	2.3	2.1-2.2	2.9-3.05	3.42	4.0	3.3	3.1	2.55

Note: W = Wurtzite; D* = Diamond; Z = Zincblende; D, I = Direct, Indirect Bandgap.

in 1968 [5], on sapphire substrates. Sapphire was selected because of its robustness with ammonia. During the 1970s, GaN research virtually ceased due to the difficulties encountered during material growth. Other issues that impeded the development were selection of a suitable substrate, controlling of the high intrinsic n-type conductivity, and obtaining conducting p-type GaN films. Nakamura et al. in 1992, discovered that annealing GaN:Mg above 750 °C in N_2 amibient converted the material to conducting *p*-type [7]. A breakthrough was once again achieved when Amano et. al. [8] reported highly improved surface morphology and optical and electrical properties of GaN films grown by Metal Organic Chemical Vapor Deposition (MOCVD) on sapphire subsrates through the use of a low-temperature (600 °C) aluminum nitride (AlN) nucleation layer. This layer is grown between the sapphire substrate and the bulk GaN film, which is typically grown at 1050 °C [8]. Advancements were also made by Nakamura (Nichia Corp., 1991) [9], by extending this concept with the introduction of a low temperature (450-600 °C) GaN nucleation layer. Currently, MOCVD is the workhorse for the growth of GaN and related materials.

GaN layers were primarily grown on sapphire substrates (Al_2O_3). Sapphire substrates offer large area availability (upto 6 inches), and good mechanical properties at low costs. The major disadvantages are its poor thermal conductivity (0.5 W/cm-K) and its large lattice mismatch to GaN which causes high defect density. Other substrates used for GaN growth are Silicon Carbide (SiC) and Silicon (Si). SiC provides smaller lattice mismatch to GaN and higher thermal conductivity compared to sapphire, which makes it suitable for high power and high temperature applications. However, the biggest disadvantage is its high cost, mediate quality and large area wafer availability. Si on the other hand, offers large area wafers at a low cost and a good thermal conductivity (1.5 W/cm-K), which make it a promising candidate for the future.

Table 2: Physical properties of substrates [25-27].

Substrate	**AlN**	**GaN**	**Al_2O_3**	**SiC**	**Si**
Thermal Conductivity [W/cmK]	3.3	1.3	0.5	3.0-3.8	1-1.5
Lattice mismatch	-2.4	-	-16	+3.5	-17
Resistivity	High	High	High	High	Medium
Cost	High	High	Low	High	Low
Wafer size [inch]	Small	Small	6	3	12

Table 2 summarizes the physical properties of the substrates. This thesis will focus on the use of sapphire due to the availability of large diameter wafers at low costs.

The advancements made in the late 1980s and early 1990s, gave rise to a renewed interest and revival of the GaN material system. For high power applications, the AlGaN/GaN HFETs have shown great potential since their first demonstration between 1991-1993. The improvements were due to higher breakdown voltage and good thermal conductivity of the HFET [59]. Eastman et. al. (Cornell), reported the use of undoped AlGaN/GaN HEMTs for power applications in [60]; Y.F. Wu et. al. (UCSB), reported the fabrication of high power density AlGaN/GaN HEMTs in [61]; and in Khan et. al. (USC) reported the observation of two-dimensional electron gas (2DEG) formation at an $Al_xGa_{1-x}N$/GaN heterojunction grown by MOCVD on sapphire [10]. GaN metal semiconductor field-effect transistor (MESFET) and heterostructure field-effect transistor (HFET) grown by MOCVD on sapphire substrates were reported in 1993 and 1994, respectively by Khan et al. [11, 12]. In 1993, Nakamura et al. demonstrated the first high-brightness (HB) blue double-heterostructure (DH) GaN LEDs [13], and in 1996, they reported the first continuous wave (CW) blue GaN LD [14].

Due to these tremendous advancements, research and commercial GaN activities have gained a lot of attention. The major concerns that need to be tackled

are producibility, reproducibility and reliability of the epitaxial material and process technologies.

Tables 3 below summarizes the major developments in GaN HFETs. Over the last decade, advancements have been made in AlGaN/GaN HFETs in terms of high breakdown voltages, high saturation currents, and low turn-on resistances. Novel structures have also been explored by various research groups. New and improved passivation layers that includes SiN_x, Al_2O_3, TiO_2, etc., have been explored. Enhancement-mode devices with high saturation currents and high breakdown voltages have been reported, as seen. The use of field-plate in improving the device performance in terms of breakdown voltage is reported in [3], and a comprehensive account of the critical geometrical and material variables controlling the field distribution under the field plate is discussed. E-mode AGaN/GaN HEMTs with integrated slant field plates is discussed in [15]. The electrical properties including the operation principle of AlGaN/GaN HFET devices are discussed in detail in [16], [17] and [62]. Various passivation techniques have been explored, and [20] reports a novel passivation technique of a combination of SiN_x and TiO_2 to reduce the surface leakage significantly. In the case of GaN based lateral devices, [21] discusses the need for a thicker epitaxial layer is preferable for suppression of vertical direction leakage current. Novel fabrication techniques for enhancement-mode HFET devices are discussed in detail in [19]. In [24], the impact of L_{gd} on the breakdown voltage performance is reported, and for the first time, mentions super-junction behavior.

This work is compared with various research groups in terms of key electrical parameters such as breakdown voltage, turn-on resistance, and zero-gate bias drain-to-source current density. Unit cell structures demonstrated a performance of over 800 V, with low turn-on resistance (of 6.1 mΩ-cm^2). The multi-fingered structures also demonstrated 800V to 1400 V of breakdown, depending on the L_{gd} value. And finally, the large area power devices exhibited a breakdown voltage of 600 V.

Table 3: Competitive study on AlGaN/GaN High Voltage HFETs.

Reference	**Substrate**	**Passivation**	**Operation**	$\boldsymbol{L_g}$ (μm)	$\boldsymbol{L_{gd}}$ (μm)	$\boldsymbol{L_{gs}}$ (μm)	$\boldsymbol{W_g}$ (μm)	$\boldsymbol{V_{th}}$ V	$\boldsymbol{R_{sheet}}$ Ω/sq.	$\boldsymbol{R_{sp}}$ Ω.cm^2	$\boldsymbol{I_{dss}}$ A/mm	$\boldsymbol{BV_{ds}}$ kV
[15]	SiC	SiN_x	D-mode	1	20	1	200	-	420	-	-	1.9
[16]	Sapphire	SiO_2	D-mode	1.5	13-16	1.5	500	-4.5	500	0.44	280	1.1
[17]	Sapphire	SiN_x	D-mode	2	20	2	100	-4.5	350	1	-	1.6
[18]	Sapphire	SiN_x+SiO_2	D-mode	1.5	10	1.5	200	-3.5	-	-	-	0.47
[19]	Silicon	SiN_x	E-mode	2	7.5	-	-	1	-	-	200	0.8
[20]	Sapphire	SiN+TiO_2	D-mode	4	28	-	50	-4	420-510	0.3	503	2
[21]	Silicon	-	D-mode	2	24	-	260 mm	-2.5	-	-	$>$ 120 A	1.8
[22]	Silicon	SiO_2	D-mode	1.5	10	-	-.2.2	15	-	-	625	1.813
[24]	Sapphire	None	D-mode	-	3-160	-	-	-	-	-	-	9
[51]	SiC	SiO_2	D-mode	-	-	-	-	-4.5	-	-	-	0.719
[52]	Sapphire	-	D-mode	-	-	-	31mm	-	-	-	$>$8 A	0.6
This Work	Sapphire	BCB	D-mode	3	15	3	300	-2.7	350	0.18	250	1.6
This Work	Sapphire	BCB	D-mode	3	25	3	5 mm	-2.7	350	0.18	$>$1 A	1.4
This Work	Sapphire	BCB	D-mode	3	15	3	40 mm	-2.7	550	0.18	$>$8 A	0.6

1.2 Application of GaN-related materials

Commercially available components consist of GaN LEDs, Laser Diodes, and HEMTs. They are used in a myriad of applications ranging from military and space to day to day applications such as displays, automobiles, etc. The major issues with GaN electronics are suitable, large area and cheap substrates for growth. Typically, Si and GaAs devices are produced on substrates of high quality, but that is not the case with GaN substrates. However, with tremendous research being done on sapphire substrates, there is a significant improvement in device performances such as high breakdown voltage and low turn-on resistance. GaN on Si substrates is also an upcoming area of research and offers a low cost, high performance platform for high power products.

As seen in Table 1, with respect to electronics, GaN is an excellent choice for high power and high temperature applications due to its high breakdown field and high saturation velocity. As a result of its wide bandgap, GaN can withstand high supply voltage, which is a key requirement for high-power device performance. Because of the high electron sheet densities (1 x 10^{13} cm^{-2}) and mobilities (1500-2000 cm^2/V-s), large drain currents can be obtained, which is another requirement for a power device. A big advantage of GaN over other compound semiconductors is the possibility to grow heterostuctures such as AlGaN/GaN. As will be seen in the later sections, the resulting two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction serves as the conductive channel.

GaN-based high power electronics have been widely used in military applications. Many defense research programs focus on the development of GaN technology for use in components such as surface radars, broadband seekers, jammers, battlefield communication, satellite communication links, transmit/receive modules, HPAs, and LNAs.

Commercially, GaN-based applications are on the verge of their breakthrough.

Other applications for GaN-based devices include switches, hybrid electric vehicles, high-voltage power rectifiers, high temperature electronics, and Hall sensors [40].

For any material to survive commercially, cost reduction is the driving factor. In order to meet this criterion, the technology must be based on a large diameter wafer, and low cost substrate material. Cost reduction can be achieved on a system level, because of GaN's high-temperture operation that eliminates the need of any additional bulky cooling units. GaN devices also require relatively lesser much off-chip circuit protection, leading to a further reduction in cost and size. And finally, the ability of GaN transistors to produce higher power densities allows the use of smaller and fewer transistors in total [37].

CHAPTER II

DEVICE DESIGN CONSIDERATIONS

2.1 Theory of Heterojunction Field Effect Transistors

The primary purpose of this thesis is to demonstrate the potential of high-voltage of AlGaN/GaN HFETs. Due to its wide energy bandgap, GaN may be suitable for high power applications in harsh environments. The most common growth direction of hexagonal GaN is normal to $(000\bar{1})$ basal plane, where the atoms are arranged in bilayers consisting of two closely spaced hexagonal layers, one with cations and the other with anions. The crystal surface of GaN can have either Ga-polarity (Ga atoms on the top) or N-polarity (N atoms on the top) [2]. As seen in Table 1, GaN has a high thermal conductivity, and a high breakdown electric field, which makes it applicable in the fields of high power and high temperature. GaN also exhibits excellent transport properties, compared to Si and GaAs.

GaN layers are grown by various methods, which gives rise to varying level of surface roughness and the quality of epilayers, and some of these methods of growth include: Metal Organic Chemical Vapor Deposition (MOCVD), Molecular Beam Epitaxy (MBE), and Hydride Vapor Phase Epitaxy (HVPE). For this work, wafers were grown using the MOCVD technique by Prof. Dupuis' group at Georgia Tech.

2.1.1 Properties of AlGaN/GaN Heterostructures

A heterojunction is formed between two semiconductors that have different energy badgap E_g. Prior to the formation of a junction, the energy band band diagram of two such semiconductors are shown in Figure 3 [2]. The energy band is formed with the lack of polarization field in semiconductors.

As can be seen from Figure 3, two semiconductors are chosen such that one has a

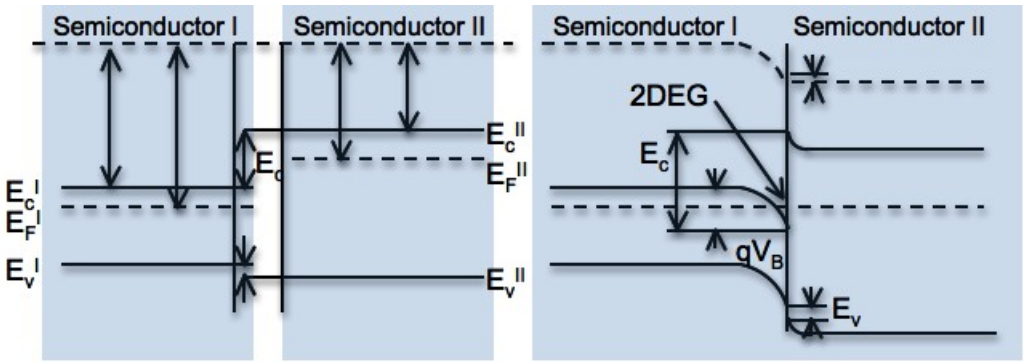


Figure 3: Energy band diagram for wide (I) and narrow (II) band gap semiconductor [2].

much wider bandgap than the other. After the two come in contact with each other, a discontinuity in the conduction band ΔE_c and valence band ΔE_v arises, which creates a triangular quantum well and near the boundary at the bottom side, a two dimensional electron gas in formed, **2DEG**.

For a typical compound semiconductor, when the heterojunction semiconductor is highly doped, the electrons are separated from the donor atoms and are collected as the 2DEG channel in the quantum well under the heterointerface. This separation of electrons from its donor atoms reduces the Coulomb scattering significantly and thus leads to a high mobility and a high saturation velocity in the channel.

The AlGaN/GaN heterostructure is created when the AlGaN barrier is grown on a thick GaN layer. Due to the difference in the bandgaps, band bending occurs and in the upper part of GaN layer near the boundary creating a 2DEG for polarization charge balance. Wurtzite group III-nitrides are tetrahedrally coordinated with a lack of symmetry along the c-direction. Due to this lack of symmetry along the c-direction along with the large ionic covalent bonds in the wurtzite GaN, a large spontaneous polarization (P_{SP}) oriented along the hexagonal c-axis occurs. The piezoelectric coefficients of III-nitrides (P_{PE}) are almost an order of magnitude larger that of conventional III-V semiconductors. So the two major sources of polarization are as follows [50]:

- Piezoelectric effect by strained AlGaN
- The spontaneous polzarization between AlGaN and GaN

The piezoelectric constants and the spontaneous polarization increase from GaN to AlN. Therefore, the piezoelectric polzarizaton of the AlGaN layer is larger than that of the GaN buffer layer, and hence a positive polarization charge is present at lower AlGaN/GaN interface, for structures with Ga-based polarity. On the other hand, for N-faced structures, a negative polarization will be compensated by holes that will be accumulated at the surface.

The tensile strength caused by the growth of $Al_xGa_{1-x}N$ on GaN reults in a piezoelectric polarization, P_{pz}, that adds to the net spontaneous polarization, P_{sp}, such that the net total polarization would be $P(x) = P_{pz} + P_{sp}$ [62], which results in a net positive charge at the AlGaN/GaN interface.

Figure 4 illustrates AlGaN/GaN based structures with Ga-polarity [50].

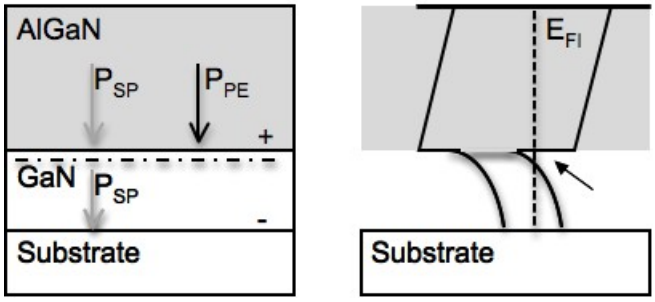


Figure 4: AlGaN/GaN based structures with Ga-polarity [50].

Due to the above mentioned polarizations in Ga-faced AlGaN/GaN heterostructures, the 2DEG can be created even without intentionally doping of the AlGaN layer. Typically, the sheet carrier concentration for such undoped structures is limited to 2 x 10^{13} cm^{-2} due to the strain relaxation of the top AlGaN layer with high Al composition.

2.1.2 Electron Transport in AlGaN/GaN Heterostructures

The electron transport model in the 2DEG channel is important. The maximum sheet charge caused by the piezoelectric polarization depends on the Al-concentration as well as on the thickness of the AlGaN layer in AlGaN/GaN heterostructures. Higher Al content can give rise to high sheet carrer density with high carrier mobility. The higher band discontinuity improves the carrier confinement and a stronger spontaneous polarization may occur, thus contributing to a higher sheet charge density in the channel.

2.1.3 III-N HFET Operation Principles

High quality III-nitride-based HFETs have been widely reported. GaN based FETs can operate under high power, high-frequency, and high-temperature conditions, that result in lower-loss and high power-switching characteristics compared to conventional devices. It is crucial to select the right substrate for better device performance.

A HFET is a three-terminal device, consisting of source (S), drain (D), and gate (G). The current between the source and the drain is controlled by the space charge which can be varied by modulating the gate. In HFETs, the current between the drain and the source flows through the 2DEG, created by electrons. The existence of the 2DEG plays an important role on the electronic transport along the AlGaN/GaN interface. The flow of electrons is controlled by the gate voltage, V_{gs}.

Figure 5 gives a cross section of an AlGaN/GaN HFET device. The source and the drain contacts are placed directly on the AlGaN layer. Ohmic contacts to the 2DEG are formed by thermal annealing. The conductivity of this 2DEG is given by the following equation [2]:

$$\sigma = q n_s \mu \tag{1}$$

where q is the electron charge, n_s is the sheet carrier concentration of free electrons, and μ is the mobility of the electrons. This shows that the channel conductivity is

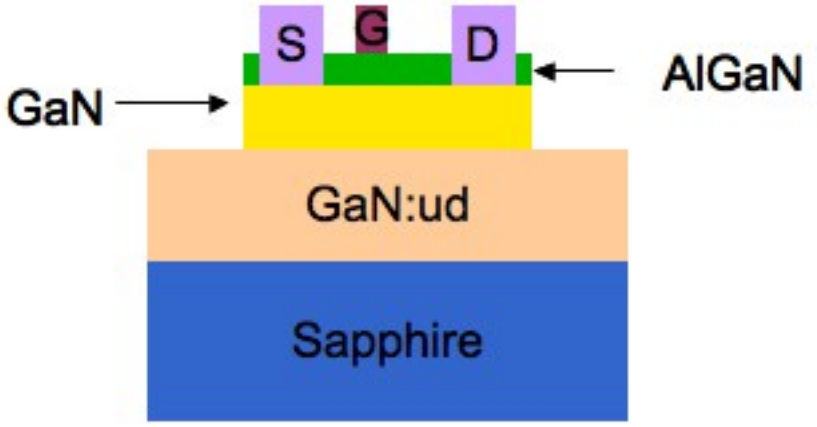


Figure 5: Cross-section of an AlGaN/GaN HFET device.

a function of the carrier concentration and the carrier mobility in electric field. The existence of the 2DEG has a critical impact on the electron transfer along the interface.

By applying a positive voltage to the drain, and the source being electrically grounded, the current flows along the 2DEG channel due to a potential drop between the source and the drain. The magnitude of current is controlled by the applied voltage to the gate contact, V_g. By applying more negative voltages on the gate, the space charge below the gate spreads towards the 2DEG with electrons. When a gate voltage is applied that is above the threshold voltage, V_{th}, electrons flow between the source and the drain. By increasing the drain bias, the drain-source current increases linearly to a certain value, also known as the *knee voltage*, after which the channel starts to saturate. The maximum saturation value of current, (I_{dss}) depends on the 2DEG. With increasing the 2DEG concentration, the I_{dss} increases [2].

2.1.4 HFET Figures of Merit

The major parameters involved in determining the DC electrical properties of HFET are:

- the saturation current, I_{dss}, given in mA/mm, at $V_{gs} = 0$V,
- the transconductance, g_m, given in mS/mm,

- the threshold voltage, V_{th}, given in olts,
- the knee voltage, V_{knee}, given in volts,
- the on-state resistance, $R_{ds(ON)}A$, given in mΩ-cm^2,
- the drain-to-source breakdown voltage, BV_{ds}, given in volts

A typical I_d-V_{ds}(I-V) relationship is shown in Figure 6(a). The curves were obtained from different V_{gs} values from -4 to 1V. This range was selected because the V_{th} was around -2.6 V for the wafers, and within this range, the on and off-state behavior can be determined accurately. The saturation current, I_{dss}, was defined at $V_{gs} = 0$V, at the onset of device saturation for D-mode devices. The knee voltage, V_{knee}, was defined as the voltage where the drain current curves with respect to the drain to source voltage transition from linear to saturation.

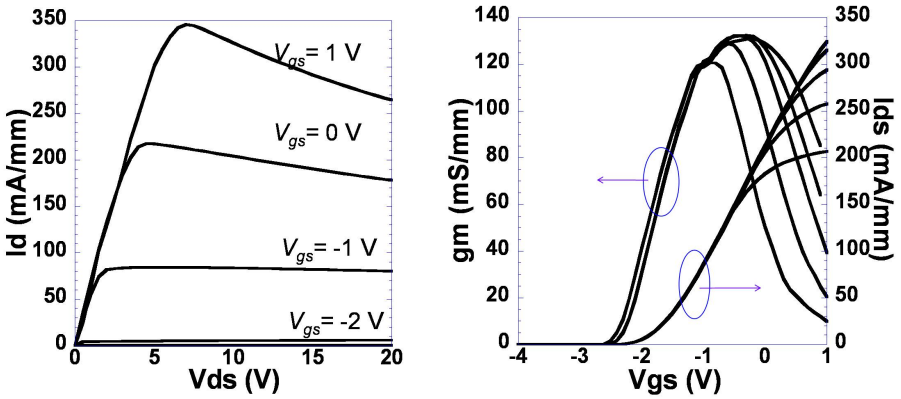
Figure 6(b) shows a typical g_m-V_{gs} relationship. From this plot, the V_{th} was determined at the region where the channel begins to turn on (-2.6V for this plot). Various I_d curves were obtained from V_{ds} between 5 - 10 V, where the channel begins to saturate.

For on-state resistance measurement, the linear region of I-V plot was assessed, at $V_{gs} = 0$V. The inverse of the slope in the linear region, multiplied by the active area of the device was equivalent to the $R_{ds(ON)}A$.

The breakdown voltage was determined at the off-state where $V_{gs} < V_{th}$. The gate voltage, V_{gs}, was modulated at -8V to -10V, and the drain leakage current was measured. For two-fingered devices, the BV_{ds} was determined when the drain current reached 1 μA (for $W_g = 300$ μm); and for multi-fingered structures, the BV_{ds} was determined when the drain current reached 10 μA (for W_g ¿ 1.5 mm).

The basic geometrical parameters of HFET are gate length (L_g) and gate width (W_g). Other important dimensions are the gate-to-source distance (L_{gs}) and gate-to-drain distance (L_{gd}). L_g determines the switching frequency limitation of the device.

The drain current flowing through the device is directly proportional to the gate width, W_g. Therefore, for power devices, large gate width is used. The devices under study in this work have W_g ranging from 0.1 mm to 40 mm.



(a) Typical I-V curves.

(b) Typical g_m curves.

Figure 6: I-V and transconductance plots obtained from a device in wafer ID: 1-1427-6 with $W_g = 300$ μm, $L_{gd} = 15$ μm, $L_g = L_{gs} = 3$ μm.

2.2 Contacts on HFETs

Besides the electronic properties of the layer structure such as carrier mobility or conductivity of 2DEG, metal contacts are important in determining the electrical properties of the device. The quality of the metal contact is crucial to stable on-state operation of the transistor switches. For example, ohmic contacts require minimal resistance so that current can pass through easily, while the Schottky contacts have to block leakage current through high barrier height [2].

2.2.1 Ohmic Contacts

By definition, an ohmic contact is referred to a contact in which the current-voltage relationship under both reverse-and forward-bias condition is linear and symmetrical. However, in reality, a contact is considered to be ohmic if the voltage drop across the metal semiconductor interface is negligible compared to the voltage drop across the bulk semiconductor [39].

The specific contact resistance and other related parameters of the ohmic contact are evaluated by the Transmission Line Model (TLM). The TLM model was first developed by Murrmann and Widmann. In this model, they considered both the semiconductor sheet resistance and the contact resistance, and described a method using linear and concentric contacts. When current flows from the semiconductor to the metal, it encounters the specific contact resistance and the sheet resistance, choosing the path of least resistance [63].

In this work, a linear array of contacts was fabricated with various spacing between them, for examples, in the order of 32, 16, 8 and 4 μm. Figure 7 below illustrates the TLM pattern used in the fabrication development of the III-N HFETs. The current flow at the contact edges significantly affects the accuracy of the contact resistance. Therefore, a mesa island was fabricated as a base for the TLM patterns, to eliminate the unwanted current flow, as shown in Figure 8 [41].

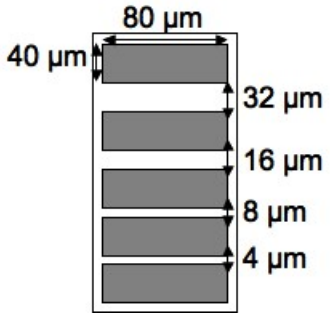


Figure 7: Schematic of TLM pattern.

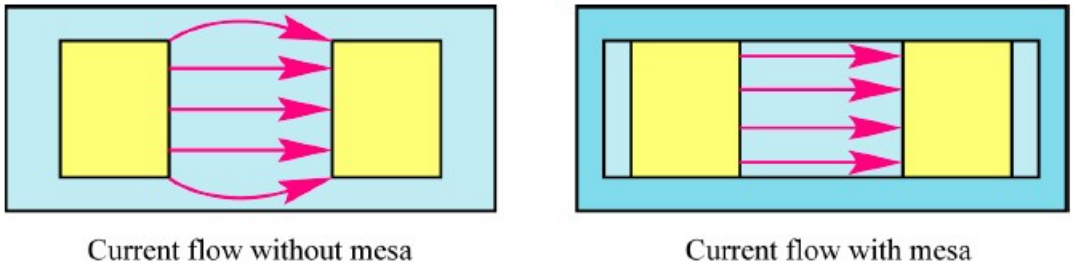


Figure 8: Current flow directions without and with mesa [41].

Assuming that the total contact resistance of one contact is R_c. Therefore, the

specific contact resistance is given by [41]:

$$\rho_c = R_c A \tag{2}$$

where A is the area of the contact.

L_T is defined as the *transfer length* within which the current transfers from the metal to the semiconductor. Thus TLM allows one to extract the specific contact resistance of a contact with lateral current flow. For each of the four spacings, I-V curves are obtained, for voltages ranging from -1V to 1V, in increments of 0.01 V/step. The resistance for each spacing is determined from the linear region of the I-V curves. These four resistances are then against the corresponding spacings, to obtain the figure shown below (Figure 9, [41]).

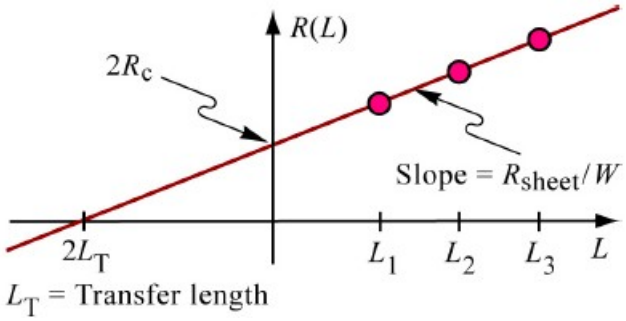


Figure 9: Resistance versus spacing of TLM patterns [41].

Assume that the semiconductor has the sheet resistance, R_{sh}. The TLM yields the following relations [41]:

$$R(L) = \frac{R_{sh}}{W} L \tag{3}$$

$$R(L=0) = 2R_c = R_{sh} \frac{2L_T}{W} \tag{4}$$

Therefore,

$$R_{sh} = \frac{R_c W}{L_T} \tag{5}$$

And specific contact resistance:

$$\rho_c = R_{sh} L_T^2 \tag{6}$$

2.2.2 Schottky Contacts

Barrier height is defined as the difference between the semiconductor conduction-band edge at the interface and the Fermi level in the metal [42]. Real and ideal I-V characteristics of a Schottky contact are schematically shown in Figure 10 [30]. The Schottky contact is characterized by the barrier height (ϕ_B), the ideality factor (η_i), the serial resistance (R_s) and the breakdown voltage (BV_{ds}). In the forward biased region, for applied voltage higher than $3kT/q$, the current is defined as [2]:

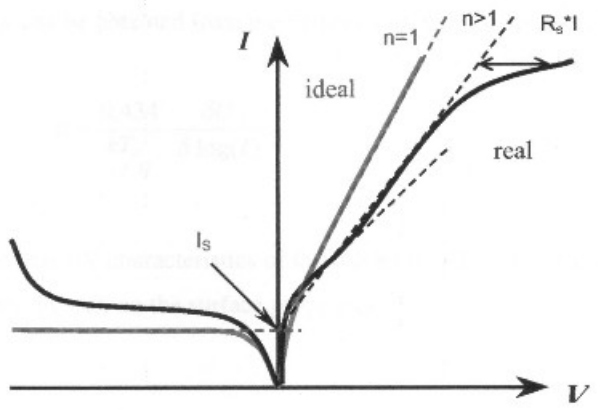


Figure 10: Real and ideal I-V characteristics of Schottky contact [41].

$$I = I_s exp(\frac{q(V - IR_s)}{nkT}) \tag{7}$$

where k is the Boltzman constant; T is the absolute temperature of the device; A is the device area; A^* is the Richardson constant, and I_s is the saturation current. The typical value for the Richardson constant is found to be in the range of 33.744 A/cm^2 K^2 [59]. A large Schottky barrier height of metal contact results in a low gate leakage current.

2.3 HFET Device Design

2.3.1 Design Goals

The design goals for the thesis were as follows:

- **High Breakdown Voltage, BV_{ds}**: Achieved by device scaling in terms of variations in gate-drain length, L_{gd}.
- **Low On-State Resistance, $R_{ds(ON)}A$**: Achieved by multi-fingered device designs and bonding pads optimization.
- **Structural Variations**: Achieved by introducing GaN cap layer (lower surface leakage), AlN binary barriers (higher I_{dss}), AlGaN composition and thickness (increased sheet charge density).

2.3.2 Unit-Cell Device Design Variation

The L_{gd} scaling was used for high breakdown voltage. For low on-state resistance, the source to gate resistance had to be minimized and this was achieved by minimizing the gate-to-source length to 2 to 3 μm. Additionally, multi-fingered devices were fabricated to reduce the resistance further since they behaved like a parallel resistance network that brought down the effective resistance. L_g variations were also introduced. The optical-contact lithography limits the resolution of the gate length to 1.5 μm. Table 4 illustrates the various design variations introduced for better device performance. Please note that the table lists values for $W_g = 300$ μm only. However, a similar approach was followed for $W_g = 200$ μm and $W_g = 400$ μm.

2.3.3 Multi-finger Device Design Variation

In addition to design variations on two-fingered devices, variations on multi-fingered devices also followed a similar approach in terms of (L_{gd}), (L_{gs}), and (L_g) variations. Extra parameters introduced were the number of fingers, and the gate width (W_g), as seen in Table 5.

Table 4: Design variations on two-fingered unit cells.

Device Type	L_g (μm)	L_{gs} (μm)	L_{gd} (μm)	W_g (μm)	Rotation (°C)
A3	2	2	8	300	-
B3	2	2	10	300	-
C3	2	2	12	300	-
D3	2	2	15	300	-
E3	2	2	25	300	-
F3	2	2	30	300	-
G3	2	2	50	300	-
H3	2	2	75	300	-
AA3	2	3	8	300	-
BB3	2	3	10	300	-
CC3	2	3	12	300	-
DD3	2	3	15	300	-
EE3	2	3	25	300	-
FF3	2	3	30	300	-
GG3	2	3	50	300	-
HH3	2	3	75	300	-
AAA3	3	3	8	300	-
BBB3	3	3	10	300	-
CCC3	3	3	12	300	-
DDD3	3	3	15	300	-
EEE3	3	3	25	300	-
FFF3	3	3	30	300	-
GGG3	3	3	50	300	-
HHH3	3	3	75	300	-
BBBR3	3	3	10	300	45
CCCR3	3	3	12	300	45
DDDR3	3	3	15	300	45
EEER3	3	3	20	300	45
BBBR3	3	3	10	300	60
CCCR3	3	3	12	300	60
DDDR3	3	3	15	300	60
EEER3	3	3	20	300	60

Table 5: Design variations on multi-fingered devices.

Device no.	**No. of fingers**	W_g (μm)	W_g (mm)	L_g (μm)	L_{gs} (μm)	L_{gd} (μm)
1	20	200	4	2	3	25
2	20	200	4	3	4	15
3	10	500	5	3	3	25
4	20	150	3	3	4	15
5	12	200	2.4	2	4	25
6	10	200	2	2	4	30
7	20	200	4	3	4	20
8	12	200	2.4	3	4	25
9	12	200	2.4	2	4	25
10	20	500	3	3	4	20
11 (Diode)	10	500	5	5	N/A	N/A

2.3.4 Circular HFETs

Mesa isolation on AlGaN/GaN material can be quite a challenge, as the etch can create pin-holes and rough sidewalls due to un-optimized processing. For quick electrical characterization of layer structures, circular HFETs were designed and fabricated. The main advantage of this type of transistor is the reduction in the number of fabrication steps. See Figure 11(a) for a typical circular HFET fabricated in this work. The fabrication consists of two lithographic and metallization steps. The gate contact is formed as a closed ring, in contrast to open fingers by rectangular or linear layout. The drain contact, which is the high current region, is placed inside the gate ring. The source metal encloses the gate ring from outside. There is no need for a mesa structure, as the source contact acts as the common (or ground) for all devices. This structure was solely used as a process control monitoring technique and to determine the wafer quality.

(a) (b)

Figure 11: (a) Circular HFET technology with $L_{gd} = 8$ μm, and (b) fingered HFET technology with $L_{gd} = 25$ μm.

2.3.5 Rectangular HFETs

For this study, a two-fingered unit cell was first fabricated, and its electrical characteristics such as breakdown voltage, saturation current, turn on resistance were studied. They were extended to form multi-fingered and large area devices. Variations in structural layers were also implemented. The W_g varied from 200 μm to 40 mm. Figure 11(b) is a typical AlGaN/GaN HFET fabricated, with $L_{gd} = 25$ μm, $L_{gs} = 3$ μm, $L_g = 3$ μm, and $W_g = 300$ μm.

CHAPTER III

DEVICE PROCESSING DEVELOPMENT

3.1 Growth and Layer Structures

The III-N HFET structures were grown in a Thomas Swan MOCVD system at Prof. Dupuis's Lab. Table 6 summarizes various structures grown for this work. The standard structure used in this work was a 20 nm AlGaN/GaN structure on sapphire substrate, and any variation in the layers were grown based on the results obtained from the 20 nm structures. Several variations were incorporated in this study. First, to increase the I_{dss}, AlN BB was introduced. Second, AlGaN thickess and Al percent composition were varied to increase the I_{dss}. Third, to reduce surface leakage and improve surface contact, a GaN cap was introduced. Fourth, to increase the sheet resistance uniformity, double-side polished wafers were grown. However, in this study, the double-side polished wafers did not show any improvement in sheet-resistance uniformity.

Figure 12(a) shows the Lehighton sheet resistance map and Figure 12(b) shows the AFM image of a standard 20 nm AlGaN/GaN HFET grown on sapphire substrate (plots obtained from Dr. Dupuis's Lab).

3.1.1 Hall and Capacitance Voltage Measurements

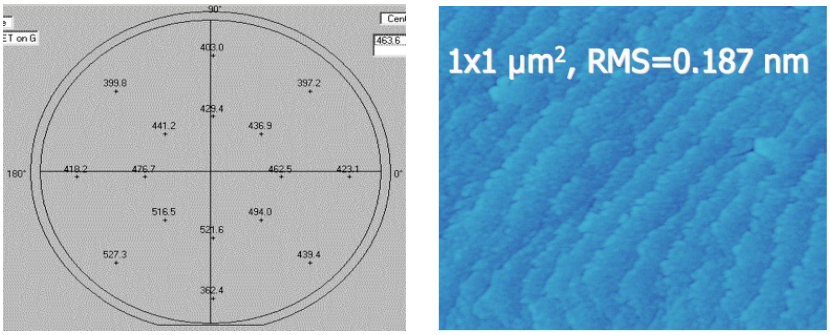
The mobility of 2DEG in HFETs is crucial for the performance of fabricated devices. Typically, Hall effect measurement is used for semiconductor characterization [58]. This method provides information about the majority type concentration and mobility.

The capacitance-voltage (CV) measurements of Schottky diode provide a quality

Table 6: Summary of structures grown for this work.

Structure	**AlGaN thickness** (nm)	**Al** %	**GaN buffer** (nm)	**GaN cap** (nm)	**AlN BB** (nm)	**Sub**	**Purpose**
I	20	25	4	-	-	SP*	Standard
II	20	25	2	-	-	SP	GaN buffer variation
III	20	25	4	2	-	SP	Improve Contact
IV	25	25	2	2	-	SP	Improve Contact
V	25	25	4	2	-	SP	Improve Contact
VI	25	25	2	2	-	SP	Buffer Variation
VII	25	25	4	2	2	SP	Improve I_{DSS}
VII	25	25	2	2	2	SP	Improve I_{DSS}
VIII	25	25	4	2	-	DP**	Uniform R_{sh}
IX	25	25	4	2	-	DP	Uniform R_{sh}
X	18	22	4	-	-	SP	Test

Note: SP, DP = Single-side polished, Double-side polished.



(a) (b)

Figure 12: (a) Lehighton sheet resistance map, and (b) AFM image of a standard 20 nm AlGaN/GaN HFET grown on sapphire substrate (Courtesy of Dr. Dupuis' Lab).

check of the heterostructure layer with 2DEG and is commonly used as a characterization method for 2DEG structures [58]. The parameters that can be evaluated from the CV measurements are concentration of 2DEG, distance of 2DEG from the surface and mobility of charge carriers.

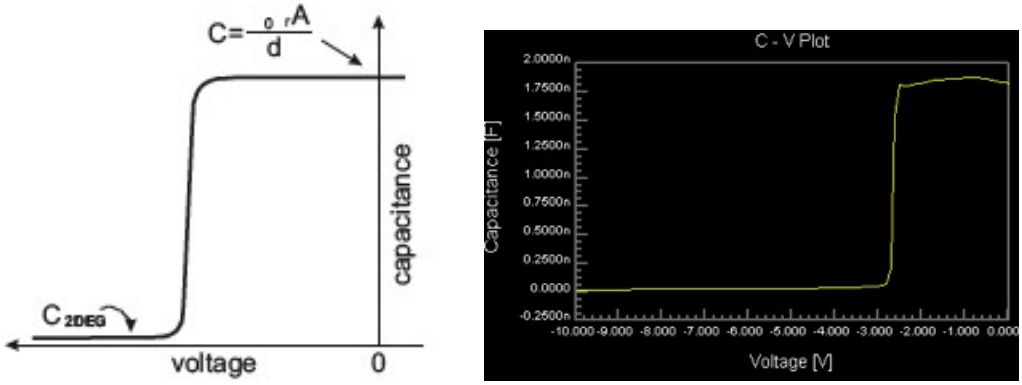
CV characteristics are measured on a diode with area A. The width of the depletion region under the Schottky contact is defined as follows:

$$w = \sqrt{\frac{2\epsilon_0\epsilon_r}{qN_d}(V_{bi} - V)} \tag{8}$$

where V_{bi} is the built-in voltage, and V is the external applied voltage. Therefore, the width of the depletion region can be controlled by the applied voltage. At zero external bias, the capacitance across the depletion space charge, with d as the distance between the Schottky contact and the 2DEG, is given as [2]:

$$C = A\frac{dQ}{dV} = A\frac{\epsilon_0\epsilon_r}{d} \tag{9}$$

Thus, at zero bias voltage, the depletion region should slightly touch the 2DEG, as seen from the above equation. Ideal CV characteristics of Schottky diode are shown in Figure 13(a), and a typical CV-characteristics from a standard 20 nm AlGaN/GaN HFET grown on sapphire substrate are shown in Figure 13(b). The typical CV-characterisitcs are obtained from Prof. Dupuis's Lab.



(a) (b)

Figure 13: (a) Ideal CV characteristics, and (b) Real CV characteristics from wafer ID 1-1427-5 (Courtesy of Dr. Hee-Jin Kim from Dr. Dupuis' group).

3.2 Device Fabrication Development

This chapter will cover the detailed fabrication steps of HFET devices starting with the mesa etching through ohmic contacts, Schottky contacts, passivation techniques, and pad metallization.

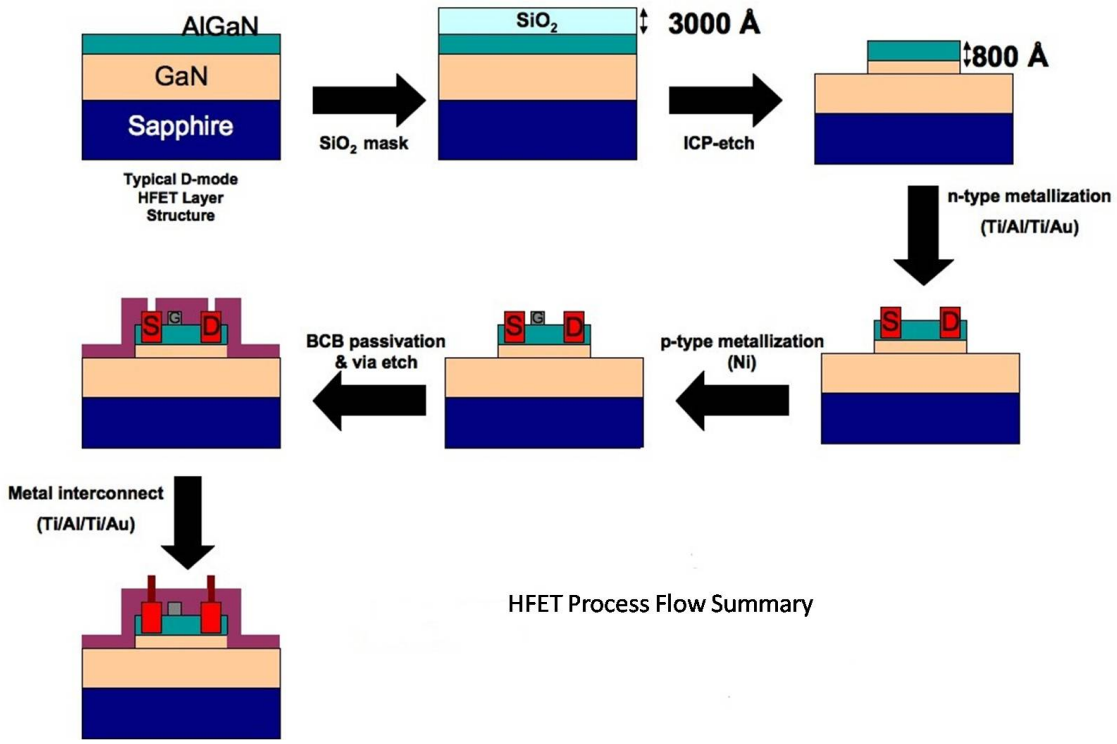


Figure 14: HFET process flow summary.

3.2.1 Process Flow Summary

Figure 14 gives an overview of the entire process flow. The first step is mesa isolation. An SiO_2 mask with a thickness of 3000 $\mathring{A}$ was used, followed by an STS-ICP etch till the GaN layer (approx. 700 $\mathring{A}$). The next step is to deposit ohmic or n-type metal comprising on Ti/Al/Ti/Au. After the metal is deposited, it has to be annealed at 850 °C for 30 seconds. The next step is to deposit gate metal, Ni. Once the ohmic and gate metals have been deposited, the surface needs to be passivated for protection from degradation. BCB passivation was used. For accessing the ohmic contacts, the BCB layer was etched in those areas using Plasma Therm ICP. Finally, thick metal (Ti/Al/Ti/Au) was deposited as interconnects.

3.2.2 Sample Preparation

GaN and AlGaN surface is unique and is also prone to dust particles and surface oxidation. Though solvent cleaning and wet etching by common acids or bases is

necessary; they are not sufficient. The GaN surface contains transparent organic and inorganic contaminants as well as native oxide. Therefore, the RCA 1 and 2 cleaning processes were performed. To begin with, the sample is placed in a dish containing H_2O_2:HCl (1:1) for 20 minutes. After stardand cleaning, the residual organic parts are removed by acetone, methanol and isopropanol. HCl-based solution is effective in removing oxides [43]. At this stage, piranha cleaning is also applied.

3.2.3 Mesa Etching

Mesa isolation provides electrical insulation between HFETs in an integrated set. The height of the mesa depends on the position of the 2DEG. Typically, for a standard structure of 20 nm AlGaN followed by 4 μm of GaN, a depth of 800-1000 $\mathring{A}$ is sufficient to get through to the 2DEG.

Optical lithography was done on Karl Suss MJB-3 Mask Aligner, and a 2-layer photo-resist was used consisting of LOR10B and S1813. The developer used was MF-319. Evaporator deposited SiO_2 mask is sufficient, but can be harmful in terms of pin-holes. The technique for etching the mesa structure was a 3000 $\mathring{A}$ oxide mask followed by an STS-ICP etched recipe using Cl_2, He and BCl_3. Satisfactory results in terms of surface smoothness have been obtained with gases relation BCl_3 (2.5 sccm)/ Cl_2 (5 sccm)/ He (32.5 sccm). The etch rate was about 10-12 $\mathring{A}$/s. The obtained sidewalls, edges and roughness of etched surface were suitable for device fabrication. Table 7 summarizes the parameters critical for the ICP plasma etch.

Due to the strong bond energy present in III-N in comparison to the other compound semiconductors, it is challenging to find the most optimal etching recipe [44]. Dry etching is advantageous in terms of providing high etch rates, anisotropic profiles [45].

Table 7: Mesa etching recipe using STS-ICP.

Parameter	Estimated values
Cl_2 (sccm)	5
BCl_3 (sccm)	2.5
He (sccm)	32.5
Coil L/T	25/50 %
Platten L/T	47/44 %
$V_{dc}(V)$	0
$V_{pp}(V)$	180
HeL (mT/min)	2-5
Power (W)	620
Time (seconds)	70

3.2.4 Ohmic Contacts

Since HFETs are large-current devices, the saturation voltage, transconductance, and other electrical properties, are sensitive to the contact resistance. It is challenging to obtain good ohmic contacts due to the existence of a high bandgap caused by AlGaN on the surface, as discussed in previous sections.

There have been many studies on the ohmic contacts on GaN and AlGaN surface [46, 47, 48, 49]. Typically, a multilayered stack is used, and as seen from literature, they have shown very good contact properties on both AlGaN and GaN layers. A study discussed in [41] demonstrated the need for a 4 layer stack consisting of Ti/Al/Ti/Au. The first layer Ti was required due to its adhesion properties and to react with the surface oxides by forming TiO_2, an oxide whose bandgap is smaller than GaN. Ti also reacts with N_2 in AlGaN and forms TiN which increases the effective carrier concentration near the surface. The second layer necessitates another metal as the formation of ohmic contacts with Ti requires very high annealing temperatures (>900 °C). Therefore a metal like Al suits the need as the interaction of Al with N_2 in AlGaN occurs at a lower temperature and results in the formation of ohmic contacts. Once Al diffuses through the surface, low resistance contact is

obtained. Diffusion takes place at a lower temperature, and then saturates. Another layer of Ti is required to form an oxygen barrier. During annealing, Al and Ti form $TiAl_3$, which acts as an oxygen barrier, inhibiting formation of surface oxides. And lastly, a fourth layer of Au is needed for low resistance contact purposes [41, 49].

All experiments were done using optical lithography, using a Karl Suss MJB3 Mask Aligner. A two-layer resist consisting of LOR 10B and S1813 was used for the gate. The developer used was MF-319. The total thickness of the resist must be at least twice that of the deposited metal for good liftoff. The ohmic metal was deposited using a CVC Electron Beam Evaporator. After literature study, and ohmic contact study (see *Results* section), Ti/Al/Ti/Au metal stack was considered most suitable for these devices. The deposition rates and thickness used were: Ti (300 $\mathring{A}$ at 2 $\mathring{A}$/s)/ Al (500 $\mathring{A}$ at 3 $\mathring{A}$/s)/ Ti (300 $\mathring{A}$ at 2 $\mathring{A}$/s)/ Au (500 $\mathring{A}$ at 3 $\mathring{A}$/s). An anneal temperature of 850 °C for 30 seconds, gave the lowest R_{sp} and R_{sh} (see *Results*).

3.2.5 Gate Metal

The gate widths of HFETs in this study were in the range of 10 nm to 40 mm. The gate lengths were in the range of 1.5 μm to 3μm. All experiments were done using optical lithography, using a Karl Suss MJB3 Mask Aligner. A two-layer resist consisting of LOR 5B and S1813 was used for the gate. The total thickness of the resist must be at least twice that of the deposited metal for smooth liftoff. The gate metal was deposited using a CHA Electron Beam Evaporator.

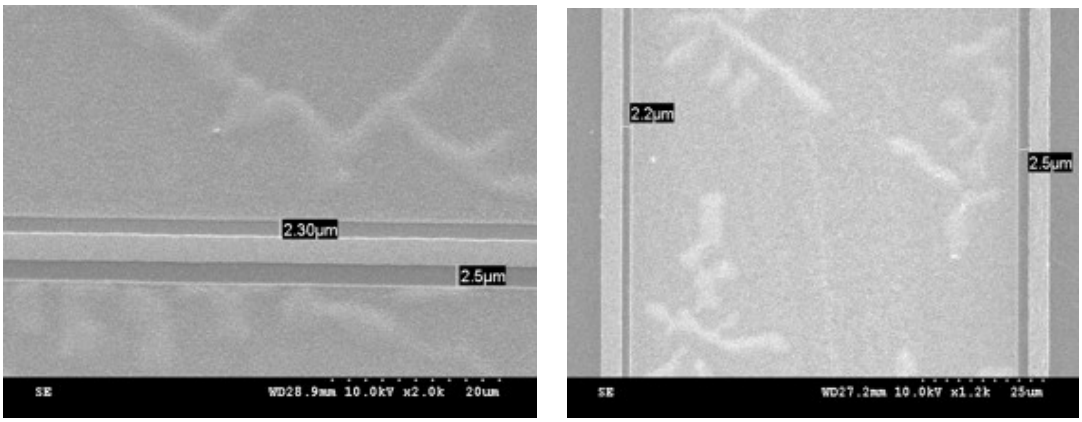
To reduce the gate metal leakage for high voltage operation in AlGaN/GaN HFETs, metals such as Au, Pt, Ni, Pd have been explored [53, 54]. Table 8 summarizes the barrier heights for various metals on GaN surface. Nickel with its large work function on GaN gives a barrier height of 0.6-1 eV [55]. It is also important for the Schottky contacts to be thermally stable for decent device operation. Typically, the Schottky metals are thermally stable between 300-600 °C [56].

Table 8: Barrier heights of metals on n-type GaN [57].

Metal	**Schottky Barrier Height** (eV)
Ni	0.95
Pt	1.01
Pd	0.94
Au	0.87

After gate metal contact study was performed, the results of which are discussed in subsequent sections, Ni gate was considered suitable choice of gate metal. The gate leakage using Ni only reduced over two orders of magnitude compared to other metal stacks explored.

Gate formation and alignment were critical for good device performance. Therefore, SEM pictures were taken for each wafer after the gate step to verify accurate gate formation and alignment. Figures 15(a) and 15(b) show the SEM pictures of a device verifying the gate alignment. After gate lift-off, a small expansion of 0.25-0.3 μm was observed, and thus, for $L_{gd} = 3$ μm, the gate to source distance was about 2.2-2.5 μm.



(a) (b)

Figure 15: SEM images of the device to verify gate formation and alignment (from wafer ID: 1-1440-6). $L_g = L_{gd} = 3$ μm.

3.2.6 Metal Pedastal and Passivation

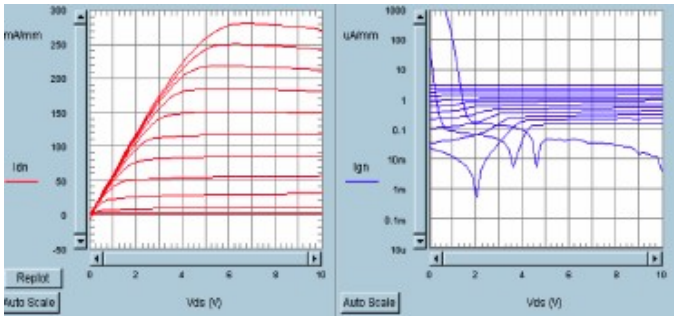
It was observed that the ohmic metal contacts degraded after the dry etching. Therefore, a metal pedestal was introduced after the gate metal processing step which included additional metal pads on the ohmic contacts and a gate bus layer to increase the thickness of the gate. The metal pedestal consisted of 300 $\mathring{A}$ of Ni and 5000 $\mathring{A}$ of Au.

To avoid the degradation of device leakage, a passivation layer was introduced. Three kinds of passivation were tested: SiN_x, Al_2O_3 and BCB. Among these, the BCB passivation was considered, due to the high process repeatability and the capability of effective reduction in leakage current by over two orders of magnitude (seen in Figure 16(a) and 16(b)). The application of BCB is extremely critical as any trace amount of O_2 affects the properties of BCB. The BCB thickness used for this work was in the range of 8000-8500 $\mathring{A}$. The curing process must be done in a vacuum oven.

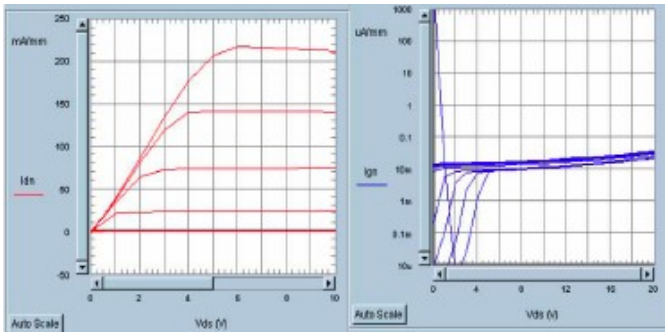
Once the BCB on the sample is cured, a single-layer photoresist photolithography step was used to pattern the via hole opening. The layer consisted of S1813, with a total thickness of 1.2 μm. The photoresist was cured for 20 minutes at 115 °C. The BCB passivation layer was etched using dry etching techniques such as Plasma-Therm ICP etch with CF_4 and Ar. After a series of experiments, it was seen that the ratio CF_4 (30 sccm)/ Ar (3 sccm) was most suitable for etching.

3.2.7 Metal Contacts

Metal contact pads are used to connect to the outside world for final measurements. For III-N HFETs in this work, contact pads with area 50 x 50 μm^2 for the small devices were used. The range of area for the large devices was from 300 x 300 μm^2 to 1000 x 2000 μm^2. Ti/Au pads with 50 nm of Ti and 750 nm of Au were used for this work, for small devices. For large area devices, Ti/Al/Ti/Au was used with 50 nm of Ti, 3.3 μm of Al, 30 nm of Ti and 50 nm of Au.



(a)



(b)

Figure 16: (a) Gate leakage suppression before passivation, and (b) gate leakage suppression after passivation.

3.3 Process Control Monitor (PCM)

At every stage of the process it is important to characterize the wafer, which can be used as check points to determine the quality of the wafer as well as the device performance. Various PCMs implemented in this work are illustrated in Figure 17, and are described as follows:

- *Transmission Line Measurements:* TLM is a technique used to determine the contact resistance between a metal and a semiconductor. By separating the metal-semiconductor contacts through various distances, the resistance between each distance is calculated by applying a voltage between the contacts and measuring the resulting currents. The measured resistance is the sum of the contact resistance of the first contact, the contact resistance of the second contact, and the sheet resistance of the semiconductor in-between the two contacts. Figure

17(a) illustrates the TLM model used in this work.

- *Alpha-step height measurement patterns:* The height of mesa, thickness of ohmic metals, gate metal, and BCB can affect the electrical performance of a device. Therefore, a PCM was essential to measure the thickness of these parameters. Figure 17(b) shows the PCM designed to measure the thicknesses, using a Tencor KLA Profilometer.

- *Mesa isolation leakage:* Mesa isolation can be a challenge in terms of fabrication and can result in under/over etch, as well as pin-holes on the surface. Therefore, PCM had to be designed to check all leakage paths associated with the mesa. Figure 17(c) shows the PCM designed to check mesa leakage.

- *Sheet resistance calculation:* In order to calculate the sheet resistance of metal contacts, a serpentine structure comprising of 350 square units was designed. This PCM was for calculating the change of resistance of the ohmic metal before/after annealing and the change of resistance of ohmic and gate metal after passivation etch. Figure 17(d) shows the PCM used for metal sheet resistance calculation.

- *Leakage paths between ohmic and gate metal:* Figure 17(e) illustrates the PCM designed to calculate the leakage paths between ohmic and gate metal layers. The PCM designed was a circular Schottky diode.

- *Via-hole chain:* After passivation etch, it was important to calculate the via access resistance, as it could affect the device performance on-state resistance of fabricated devices. Therefore, a via chain was designed with 10 μm by 10 μm square units. (Figure 17(f)).

- *Vernier scale:* A set of vernier scales were used to gauge the alignment errors, as seen in Figure 17(g).

- *Quick test devices:* A few single-fingered quick test devices were introduced, that consisted of a single-finger gate, and $L_{gs} = L_{gd}$ in the range of 2, 3 4 and 5 μm. These were quick test devices that helped test various threshold voltage and resistance characteristics of the wafer (see Figure 17(h)).

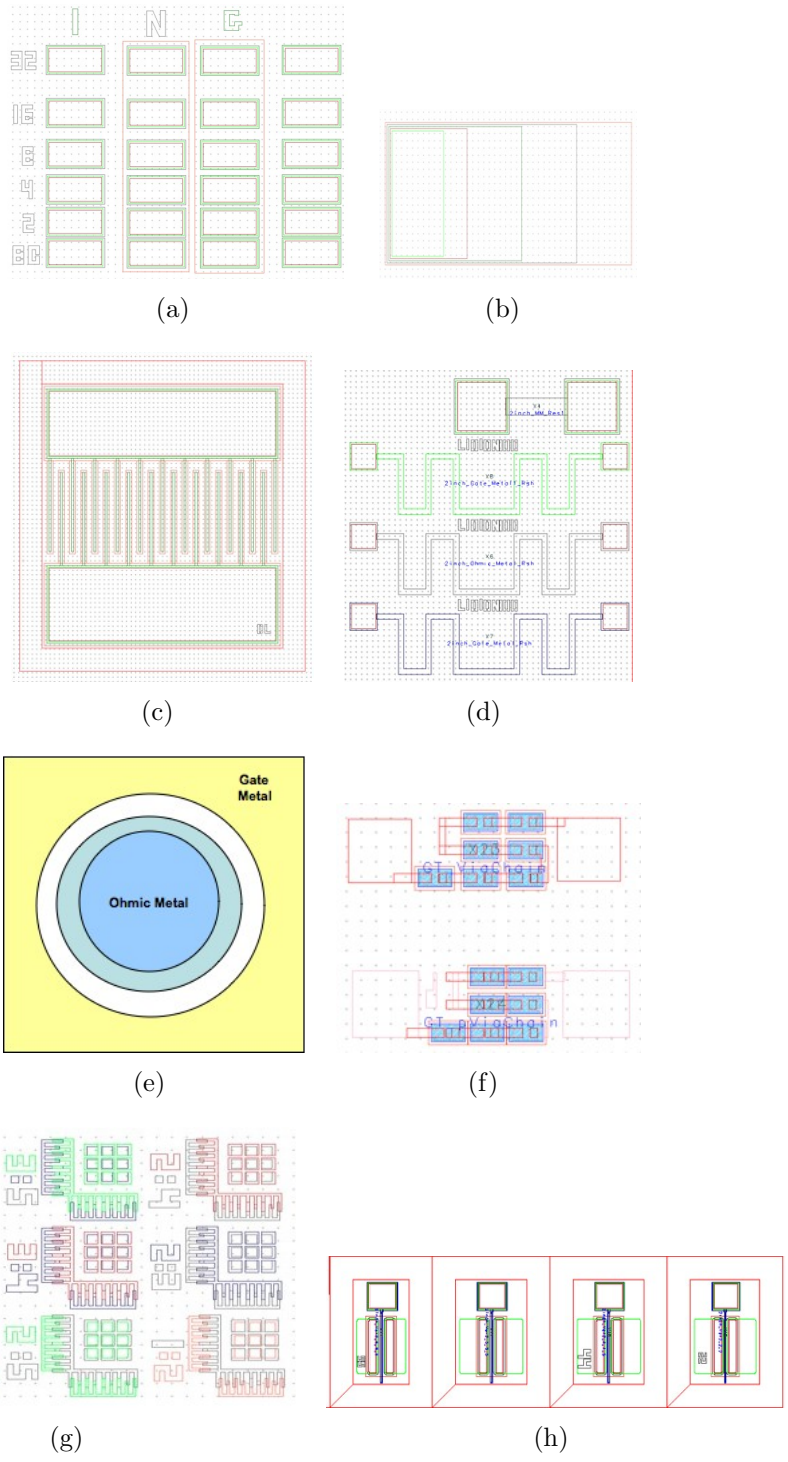


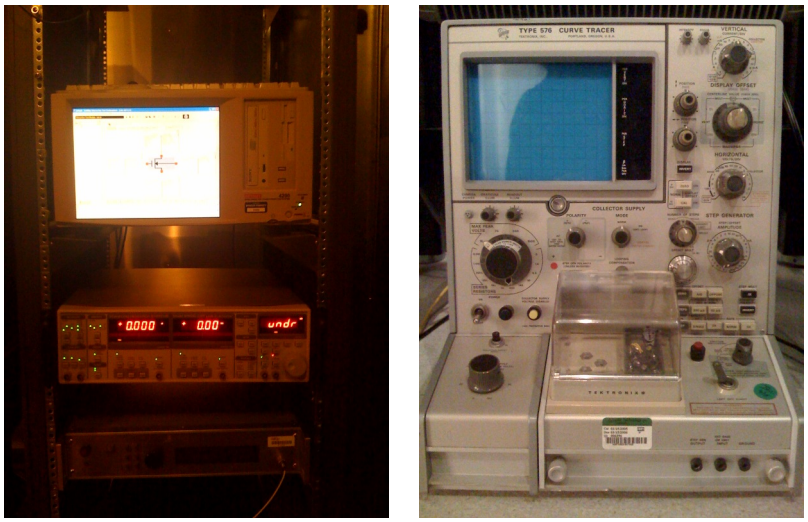
Figure 17: (a) shows the Transmission Line Measurements designed for this work, (b) shows the PCM that aided in mesa height check to ensure the etching was uniform, (c) shows the PCM used to check the leakage current due to the mesa isolation, (d) shows the PCM used to calculate the sheet resistance, (e) shows the PCM used to check the leakage between ohmic on the mesa and the gate metal, (f) shows the PCM used to calculate the via access resistance, (g) shows the PCM helped check alignment, and (h) shows the single-fingered test devices with $L_{gd} = L_{gs} = 2$, 3, 4 and 5 μm that helped check device performance after the gate metal.

CHAPTER IV

RESULTS AND DISCUSSION

4.1 Characterization

The equipment used for characterization were Keithley 4200 and Textronix Curve Tracer Type 576, shown in Figure 18(a) and (b), respectively. For high voltage measurements, the sample was placed in fluorinert (solution type FC-9) to avoid arching and other issues.



(a) (b)

Figure 18: Instruments used for characterization of high-power HFETs, (a) Keithley 4200 and (b) Tektronix Curve Tracer.

Wafer pieces approximately 1.5 cm by 1.5 cm were used for the fabrication of two-fingered unit cell devices. Once the process was optimized based on parameters such as turn-on resistance, breakdown voltage, and gate leakage current, fabrication was performed on 2-inch wafers, and statistical data was obtained for all wafers.

For each device, the following parameters were evaluated: sheet resistance (R_{sh}), specific contact resistance (R_{sp}), saturation current (I_{dss}), transconductance (g_m),

threshold voltage (V_{th}), turn-on resistance ($R_{ds(ON)}A$), and breakdown voltage (BV_{ds}).

4.2 Structural Variations

A series of structural variations were introduced in order to improve certain properties such as reduction in surface leakage, uniform sheet resistance, and increase in I_{dss}. Standard structure includes a 20 nm AlGaN (25%), 4 μm GaN, on sapphire. However, this structure did not give the desired I_{dss} of 0.3 A/mm or higher and hence AlN Binary Barrier was introduced, as well as Al composition in terms of AlGaN thickness and percent composition were varied. GaN cap was introduced to lower the surface leakage and form good contacts with the surface. Table 9 gives a list of wafers fabricated along with layer structures used for this work.

Figure 19 contains microscopic images of two-fingered and multi-fingered devices fabricated in this work. 19(a) and (b) show the fabricated two-fingered device, and the design variation performed on the two-fingered devices. Figure 19(c) and (d) show the multi-fingered structures of W_g of 4 and 2.4 mm. Figure 19 (e) shows the fabricated multi-fingered device with W_g of 5 mm, and Figure 19 (f) shows a part of the large area device with W_g of 40 mm.

4.3 ICP Dry Etching Study

It is essential to evaluate the process at every stage. There are six photolithography steps for this process: Mesa Isolation, Ohmic, Gate, Metal Pedestal, BCB Via, and Metal-1. For each step, the PCM was evaluated, the results of which are reported in this section.

It is crucial to have accurate mesa heights for the isolation layer. The targeted value is between 700-900 $\mathring{A}$. As mentioned previously, a PCM was designed to calculate the mesa height using a Tencor KLA Profilometer. Typical measurement results are shown below. Figure 20(a) provides the distribution of heights across the wafer. Figure 20(b) contains the sheet resistance map as obtained from the growers. Figure

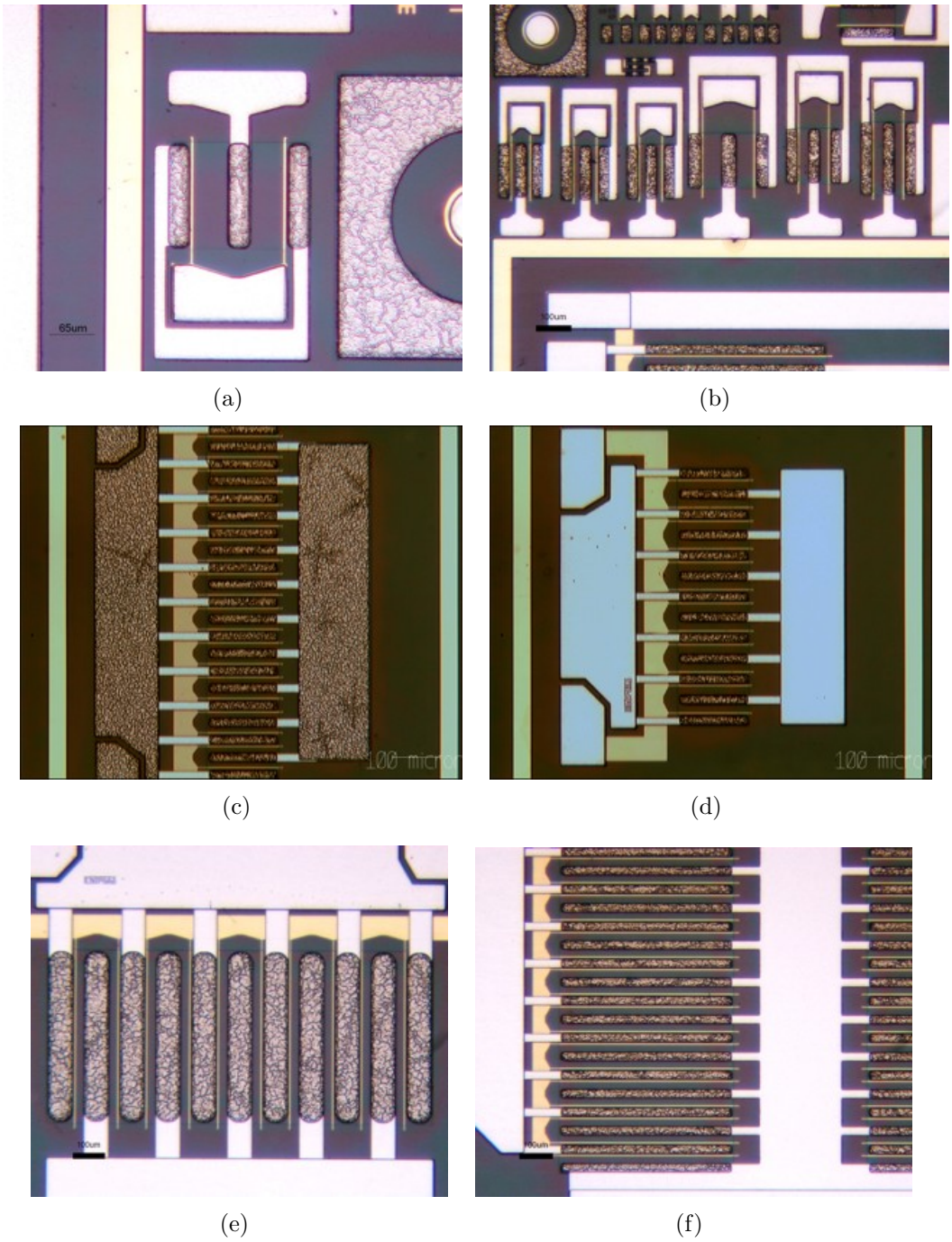
Table 9: Wafers grown and fabricated with different layer structures.

Wafer ID	**AlGaN** (nm)	**Al** (%)	**AlN BB** (nm)	**GaN cap** (nm)	**Substrate**
1-1410-6	18	22	-	-	Single-side polished
1-1421-6	18	22	-	-	Single-side polished
1-1425-6	20	22	-	-	Single-side polished
1-1427-1	20	25	-	-	Single-side polished
1-1438-6	20	25	-	2	Single-side polished
1-1439-6	25	25	-	2	Single-side polished
1-1440-6	25	25	-	2	Single-side polished
1-1479-6	25	25	1	2	Single-side polished
1-1531-6	25	25	-	2	GaN:Fe template
1-1532-1,6	25	25	-	2	Single-side polished
1-1532-2	25	25	-	2	Double-side polished
1-1533-6	25	25	-	2	GaN:Fe template
1-1534-1,6	25	25	1	2	Single-side polished
1-1534-2	25	25	1	2	Double-side polished
1-1534-5	25	25	1	2	Single-side polished
1-1536-1,6	25	25	-	2	Single-side polished
1-1536-2	25	25	-	2	Double-side polished
1-1639-1,2	20	25	-	-	Single-side polished
1-1643-1,2	20	25	-	-	Single-side polished

Note: All wafers were grown on sapphire substrates.

20(c) give the statistical distribution of the mesa height on a 2-inch wafer.

After ohmic metal is deposited, TLM data was measured. The ohmic metal used in this study was Ti (300 $\mathring{A}$) / Al (500 $\mathring{A}$) / Ti (300 $\mathring{A}$) / Au (500 $\mathring{A}$). Statistics of TLM measurements and it's corresponding mapping with the sheet resistance was recorded. Figure 21 provides information about the statistical distribution of TLM typically observed in the wafers.

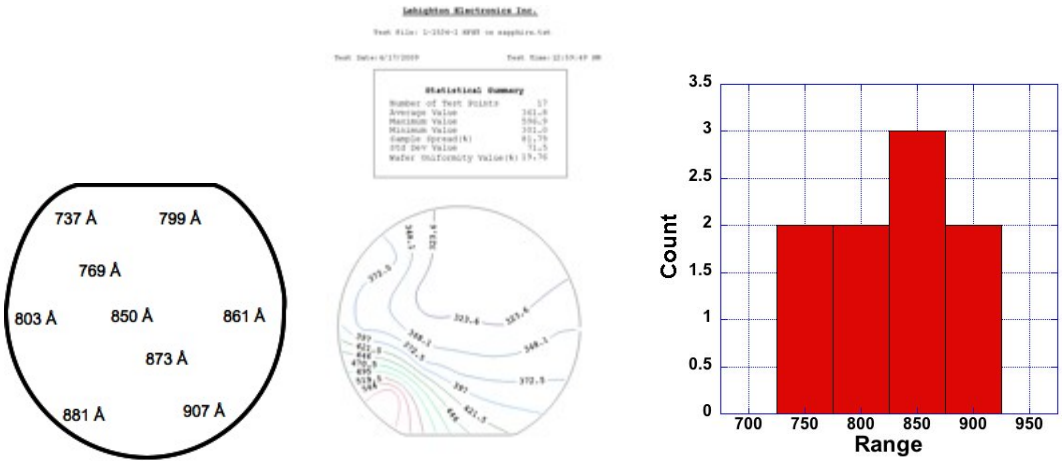


(a) (b)

(c) (d)

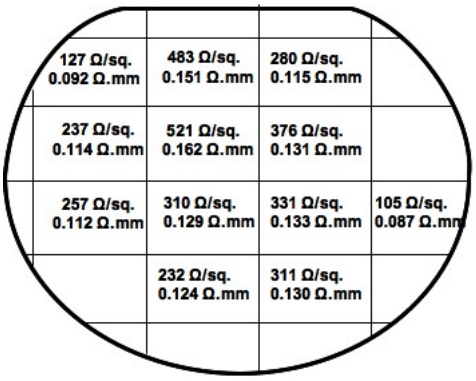
(e) (f)

Figure 19: Unit cell structures and multi-fingered structures fabricated. (a) is a two fingered unit cell device. (b) is a set of design variations to the two-fingered devices to test parameters such as breakdown voltage, I_{dss}, and turn-on resistance . (c) is a multi-fingered device with $W_g = 4$ mm. (d) is a multi-fingered device with $W_g = 2.4$ mm. (e) is a multi-fingered device with W_g =5mm. (f) is a multi-fingered structure with $W_g = 40$ mm.

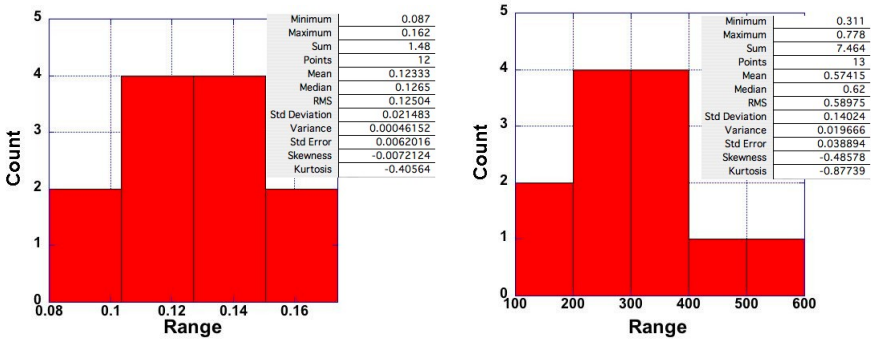


(a) (b) (c)

Figure 20: (a) Mesa height data obtained from wafer ID: 1-1535-1, (b) sheet resistance map(obtained from Dr. Dupuis's Lab), and (c) statistical distribution of the mesa height.



(a)



(b) (c)

Figure 21: (a) Sheet and specific contact resistance distribution from wafer ID: 1-1535-1, (b) sheet resistance statistical distribution, and (c) specific contact resistance distribution.

4.4 Ohmic and Gate Metal Study

4.4.1 Ohmic Contact Study

For this study, Ti/Al/Ti/Au was used as a metal stack, and different annealing temperatures were tested, based on literature [46]. After the ohmic metal study, it was concluded that a thickness of Ti (300 $\mathring{A}$)/ Al(500 $\mathring{A}$)/ Ti(300 $\mathring{A}$)/ Au (500 $\mathring{A}$) was optimal based on TLM measurements and ohmic metal morphology. Various experiments were conducted to estimate the right annealing temperature. Tables 10 and 11 summarize the results of the study, in terms of surface smoothness, and R_{sh} and R_{sp}. As seen from the table, at 850 °C the anneal temperature gave the lowest specific contact resistance.

4.4.2 Gate Metal Study

In order to determine the right metal layer, a variation was introduced in the gate metal stack. The gate metal variation experiment was performed on wafer ID 1-1531-6. The 2-inch wafer was cut into four pieces of approximately the same size. Apart from gate metal, all other steps involved in the process were kept constant, and the four pieces were processed together. Following were the metal compositions used: Ni (2000 $\mathring{A}$); Ni (1000 $\mathring{A}$)/ Au (1000 $\mathring{A}$); Ni (300 $\mathring{A}$)/ Pd (1500 $\mathring{A}$); Ni (300 $\mathring{A}$)/ Pt (1500 $\mathring{A}$). Table 12 compares the results obtained from the various pieces. The device specifications are as follows: **Wafer ID**: 1-1531-6; L_g=3μm, L_{gs}=3μm, L_{gd}=15μm, W_g=300μm. Table 13 below summarizes key results needed for gate metal evaluation obtained from the plots in Table 12.

As seen from Table 13, the gate leakage for the piece with Ni only gate metal was superior to that from other metal stacks, reducing the leakage current by nearly two orders of magnitude, comparatively. A few high voltage measurements were performed in order to verify device performance, and Figure 21 discusses the results from the measurements, comparing Ni with Ni/Au. Figure 22(a) and (b) shows the

Table 10: Optimization of anneal temperature.

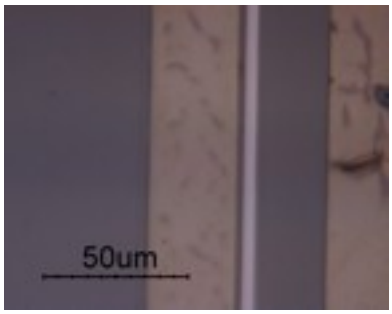
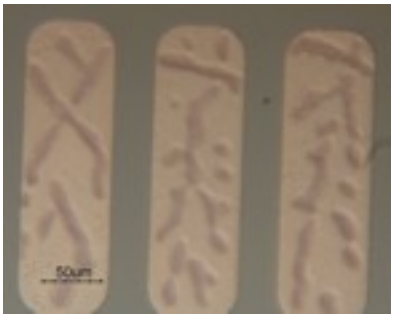
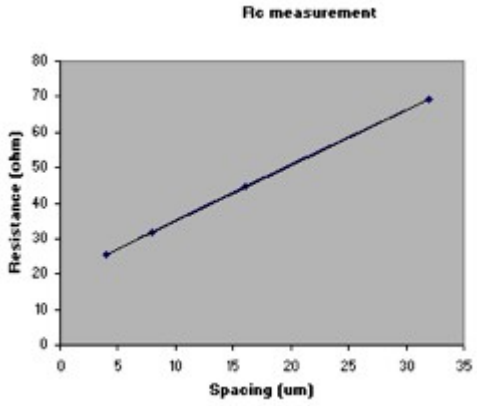
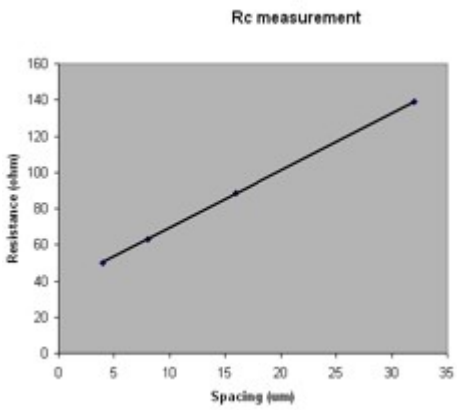
Anneal Temperature: 700 °C Time: 1 minute	**Anneal Temperature: 750 °C Time: 1 minute**
	
	
R_{sh} = 327 Ω/sq. ρ_c = 1.7 x 10^{-3}Ω/-m^2	R_{sh} = 327 Ω/sq. ρ_c = 4.6 x 10^{-4}Ω-cm^2

Table 11: Optimization of anneal temperature.

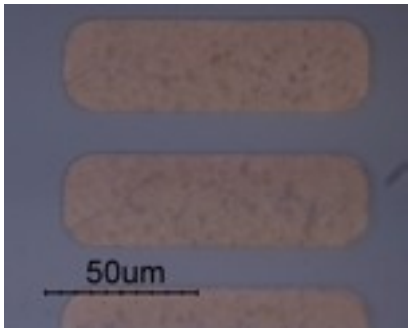
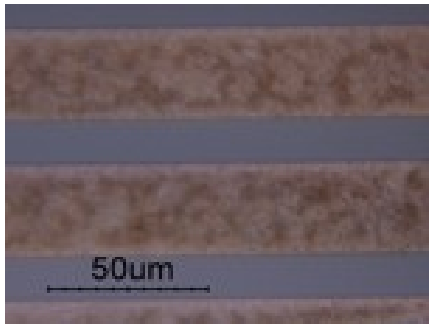
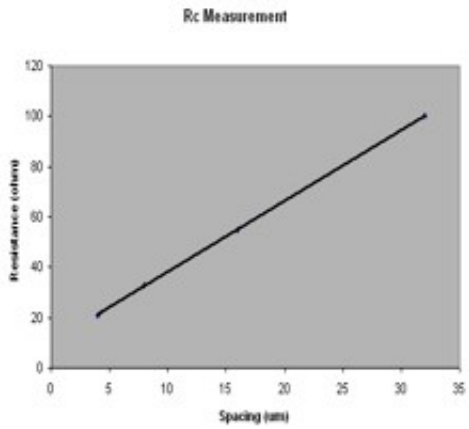
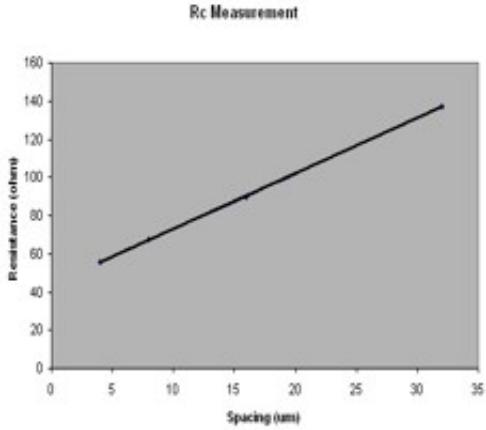
Anneal Temperature: 800 °C **Time: 1 minute**	**Anneal Temperature: 850 °C** **Time: 30 seconds**
	
	
R_{sh} = 327 Ω/sq. ρ_c = 1.1 x 10^{-4}Ω-cm^2	R_{sh} = 327 Ω/sq. ρ_c = 6.7 x 10^{-5}Ω-cm^2

Table 12: Gate metal variation study (Device dimensions: **Wafer ID**: 1-1531-6; L_g=3μm, L_{gs}=3μm, L_{gd}=15μm, W_g=300μm).

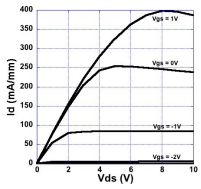
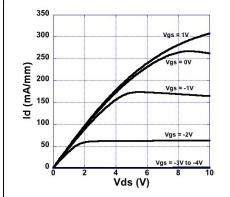
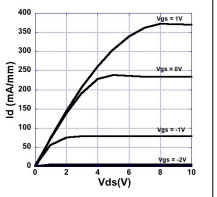
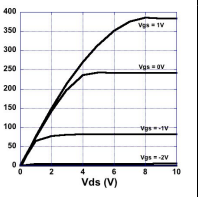
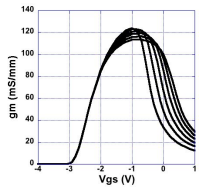
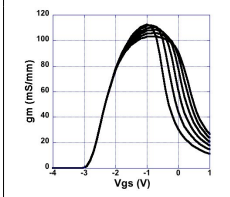
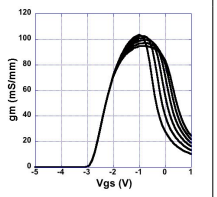
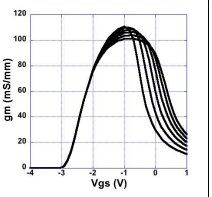
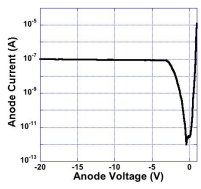
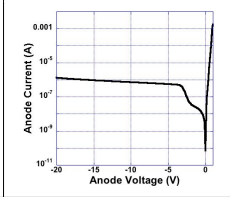
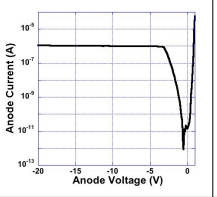
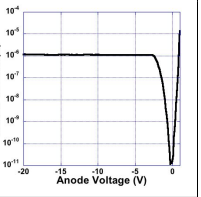
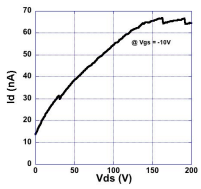
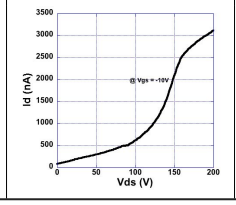
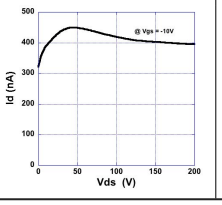
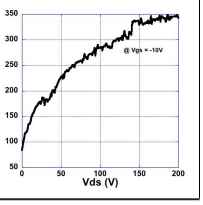
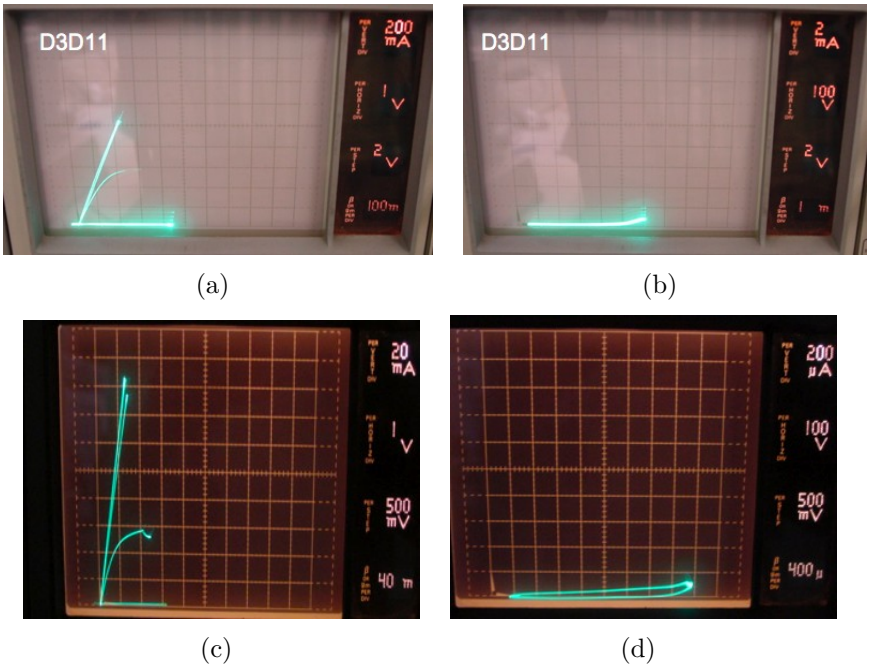
Characteristics	Ni	Ni/Au	Ni/Pd	Ni/Pt
I-V analysis V_{ds}: 0-10V V_{gs}: -4 to 1V				
gm analysis V_{ds}: 5-10 V V_{gs}: -4-1V				
GD diode Rev: -20-1V				
HV analysis V_{ds}: 0-200V V_{gs}: -10V				

Table 13: Important results from gate metal variation study (Device dimensions: **Wafer ID**: 1-1531-6; L_g=3μm, L_{gs}=3μm, L_{gd}=15μm, W_g=300μm).

Gate metal	$\boldsymbol{I_{dss}}$ @ V_{gs} = 0V *(mA/mm)*	$\boldsymbol{g_{m,max}}$ *(mS/mm)*	**Gate Leakage** @ V_{gs} = -10V *(A)*	**Drain Leakage** @ V_{gs} = -10V *(nA)*
Ni	250	120	10^{-7}	65
Ni/Au	175	115	8x10^{-5}	3000
Ni/Pd	235	101	10^{-6}*	400
Ni/Pt	247	107	10^{-6}*	350

*= Does not hit compliance. It is the value obtained from the real curves.

high leakage characteristics observed with Ni (1000 $\mathring{A}$)/ Au (1000 $\mathring{A}$), while Figure 22(c) and (d) shows the low leakage characteristics (in the order of 10 nA) observed with Ni (2000 $\mathring{A}$).



(a) (b)

(c) (d)

Figure 22: Gate metal variation: High voltage study.

Wafer ID: 1-1534-1 for Ni; 1-1536-6 for Ni/Au; L_g=L_{gs}=3μm, L_{gd}=20μm, W_g=40 mm. (a) shows device with Ni/Au gate metal, (b) shows the corresponding breakdown voltage plot with $BV_{ds} < 600$ V, (c) shows device with Ni-only gate metal, and (d) shows the corresponding breakdown voltage plot with $BV_{ds} > 900$ V.

As seen the leakage characteristics of Ni only gate metal is over two order of magnitude less than that seen in Ni/Au gate metal device. Therefore, Ni was selected as the gate metal for the process. A challenge seen here was the deposition of the metal, as Ni has a tendency to peel after evaporation due to its high stress properties. This issue was resolved by using an appropriate deposition rate of 3 $\mathring{A}$/s for a total thickness of 2000 $\mathring{A}$.

4.5 Two-fingered Unit Cells

First, two-fingered unit cell devices were designed and fabricated. Then, a design variation was introduced on the unit cells, as discussed in the previous section.

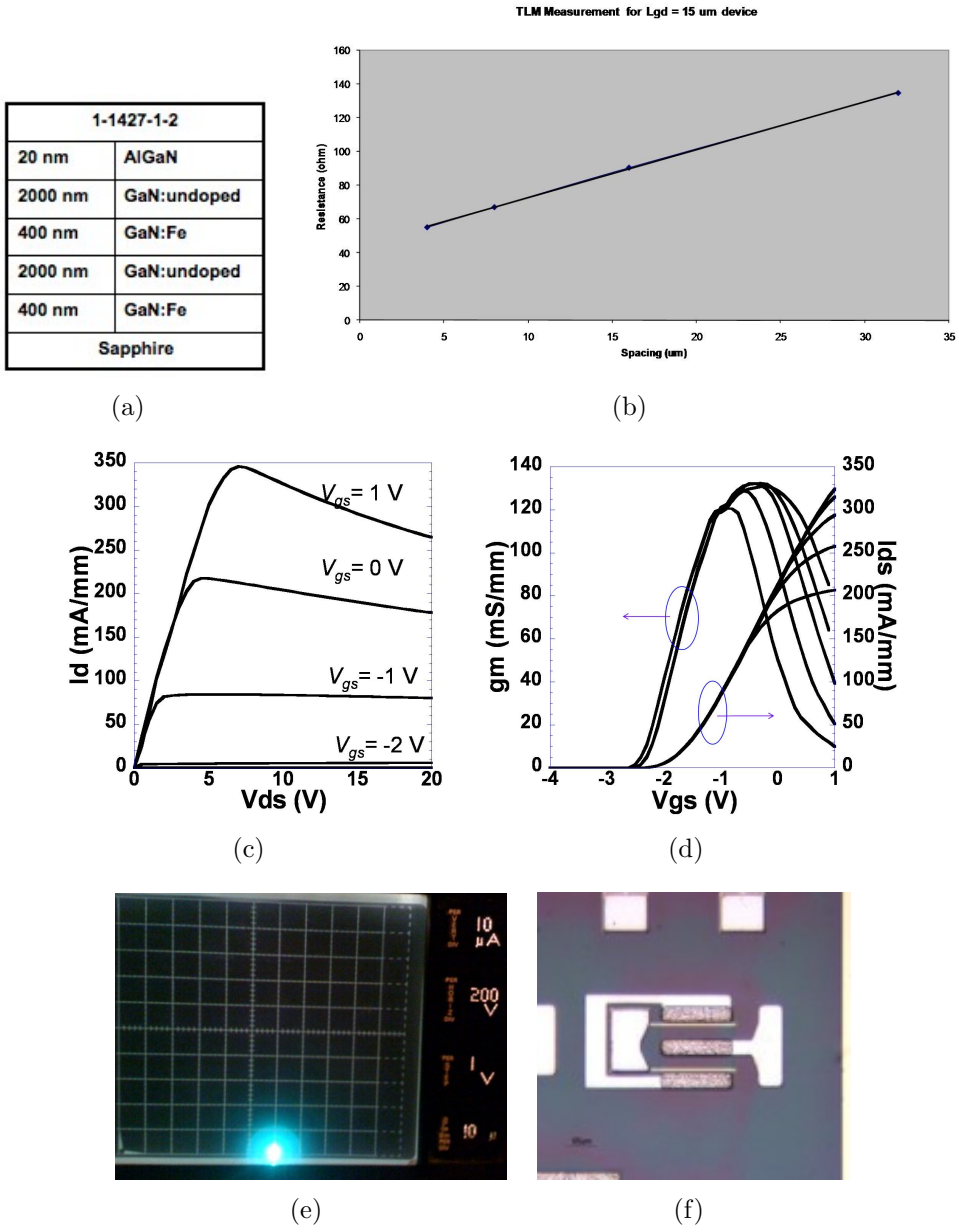


Figure 23: Two-fingered unit cell power HFET device: W_g = 300 μm, L_g = 3 μm, L_{gs} = 3 μm, L_{gd} = 15 μm. (a) shows the wafer structure, (b) shown the sheet and specific contact resistance graph (R_{sh} = 327 Ω/sq.; R_{sp} = 8.8 x 10^{-5} Ω-cm^2), (c) shows the I-V curves for the device, (d) shows the I_d, gm curves, (e) shows the breakdown voltage of the device (BV_{ds} = 1.2 kV), and (f) shows a microscopic image of the device.

For each of the devices fabricated, common-source I-V curves, transconductance, turn-on resistance, and breakdown voltage were obtained. Figure 23 summarizes the results obtained from L_{gd} = *15* μm devices, as observed on standard structure wafers (ID: 1-1427-1). The turn-on resistance was estimated to be $R_{ds(ON)}A = 6.5$ mΩ-cm^2. At $V_{gs} = 0$V, I_{dss} was 220 mA/mm, g_m was 120 mS/mm, and V_{th} , was -2.6V. The breakdown voltage was 1.2 kV.

Table 14 summarizes the performance of various L_{gd} devices obtained from wafer ID: 1-1427-1. Statistical data was obtained after measuring six devices of a similar kind. The BV_{ds} is greater than 700 V for all devices; and for $L_{gd} > 50$ mm the devices' breakdown voltage is well above 1.6 kV.

Table 14: Summary of two-fingered devices (1-1427-1).

$\boldsymbol{L_{gd}}$	$\boldsymbol{V_{th}}$		$\boldsymbol{I_{dss}}$		$\boldsymbol{gm_{max}}$		$\boldsymbol{R_{ds(ON)A}}$		$\boldsymbol{BV_{ds}}$
(μm)	(V)	σ	(mA/mm)	σ	(mS/mm)	σ	mΩ-cm^2	σ	(kV)
10	-2.21	0.23	222	1.33	132.3	0.76	6.1	2.11	0.7
15	-2.3	0.61	210	0.87	128.8	0.93	6.5	1.35	1.2
25	-2.28	0.17	195.7	2.09	98.5	1.21	7.3	0.91	1.400
30	-2.21	0.34	192.4	2.45	96.2	0.56	9.5	2.91	1.6
50	-2.21	0.41	189.2	0.49	89.4	1.75	11.23	1.18	>1.6
75	-2.27	0.52	187.1	2.63	87	2.06	13.11	3.11	>1.6

Variations in structural layers impacted the device performance significantly. Figure 24 summarizes the device data obtained from different wafers, for $L_{gd} = 25$ μm. In terms of breakdown voltage, standard structure (1-1427-1), and low Al content structure (1-1410-6) showed a reduction in drain leakage by an order of magnitude compared to other structures. In terms of I_{dss}, higher Al content wafers (1-1439-6 and 1-1535-5) performed better (increase in saturation current by nearly 20%). Devices with GaN cap exhibited a low $R_{ds(ON)}$.

Table 15 lists key results from all wafers fabricated. The dimensions of the device type for evaluation has $L_g = 3$ μm, $L_{gs} = 3$ μm, $L_g = 15$ μm, $W_g = 300$ μm. The

comments section of the table lists a brief explanation on the device performance. *Good performance* indicates low turn-on resistance (<0.1 ohm/mm), high breakdown voltage (> 800 V), and low gate leakage (I_g < 100 n).

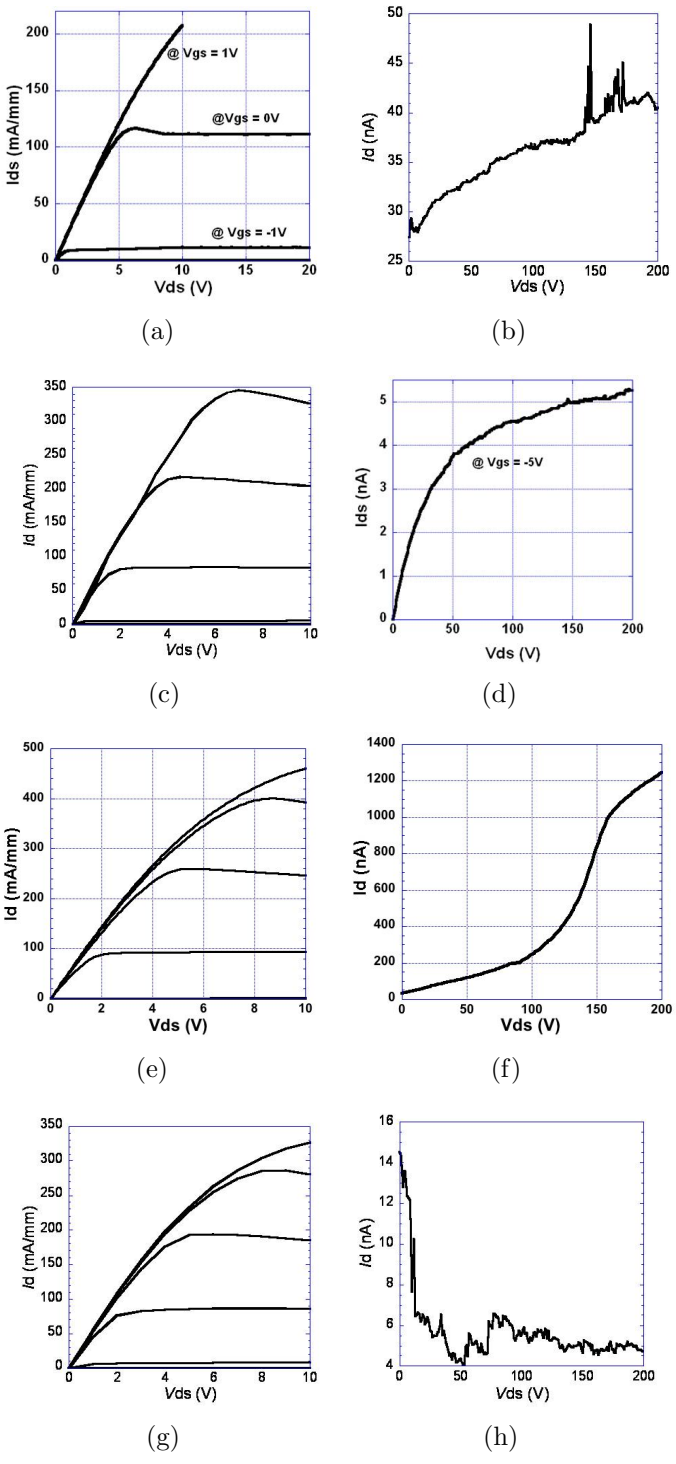


Figure 24: Device: $W_g = 300$ μm, $L_g = 3$ μm, $L_{gs} = 3$ μm, $L_{gd} = 25$ μm. (a) shows I-V curves for typical device (Type X in Table 6), (b) shows Drain leakage @ 200 V at V_{gs} = -5V, (c) shows I-V curves for typical device (Type I in Table 6), (d) shows Drain leakage @ 200 V at V_{gs} = -5V, (e) shows I-V curves for typical device (Type VII in Table 6), (f) shows Drain leakage @ 200 V at V_{gs} = -5V, (g) shows I-V curves for typical device (Type IV in Table 6), and (h) shows Drain leakage @ 200 V at V_{gs} = -5V.

Table 15: Summary of W_{gd} = 300 μm, L_{gd} = 15 μm, L_{g2} = 2 μm devices fabricated on different wafers.

Wafer ID	ρ_c (Ω-cm^2)		$\boldsymbol{R_{sh}}$ (Ω/sq.)		$\boldsymbol{R_{ds(ON)A}}$ (mΩ-cm^2)		$\boldsymbol{I_{dss}}$ (A)		**Leakage** (A)	$\boldsymbol{V_{th}}$ (V)		**Comments**
	Avg.	Dev.	Avg.	Dev.	Avg.	Dev.	Avg.	Dev.	Avg.	Avg.	Dev.	
1-1410-6	9.2 x 10^{-5}	1.02	370	132	23.21	3.03	0.22	0.054	222 n	-1.5	0.026	Good performance
1-1421-6	1.00 x 10^{-4}	3.05	202	169	32.31	1.36	0.18	0.056	312 n	-1.7	0.0421	Good performance
1-1425-6	1.63 x 10^{-5}	3.71	221	252	26.89	5.43	0.26	0.041	150 μ	-2.2	0.0313	Large I_g
1-1427-1	6.6 x 10^{-5}	1.16	307	57	6.5	7.62	0.222	0.06	39 n	-2.3	0.0162	Champion Device
1-1428-5	8.97 x 10^{-5}	1.23	330	91	17.91	8.36	0.210	0.031	63 n	-2.218	0.0206	Good performance
1-1438-6	5.4 x 10^{-5}	1.07	333	41	17.03	3.62	0.32	0.053	189 n	-2.7	0.0402	Good I_{dss}, large I_g
1-1439-6	4.7 x 10^{-5}	3.30	350	75	13.65	2.19	0.34	0.0288	236 n	-2.71	0.0562	Good I_{dss}, large I_g
1-1440-6	7.3 x 10^{-5}	4.61	295	60	19.13	2.78	0.29	0.0463	172 n	-2.65	0.0342	Good I_{dss}, large I_g
1-1479-1	2.70 x 10^{-6}	2.71	597	172	16.23	2.27	0.44	0.0636	1 m	-2.7	0.0121	Large I_g , Ni/Au gate
1-1531-6	6.70 x 10^{-5}	1.09	230	57	25.15	2.01	0.29	0.0127	64 n	-2.91	0.0501	Low I_g , Ni gate
1-1532-1	1.07 x 10^{-5}	6.4	691	107	21.42	5.21	0.42	0.0678	1 m	-2.4	0.0451	Large I_g , Ni/Au gate
1-1532-2	5.1 x 10^{-5}	2.61	337	63	21.4	2.98	0.27	0.0203	414 n	-2.5	0.0513	Large I_g , Ni/Au gate
1-1532-6	2.02 x 10^{-6}	4.53	541	236	19.56	1.05	0.35	0.0215	1 m	-2.4	0.0517	Large I_g , Ni/Au gate
1-1534-1	9.00 x 10^{-7}	2.1	608	197	17.89	2.78	0.38	0.0778	1 m	-3.313	0.0671	Large I_g , Ni/Au gate
1-1534-2	2.4 x 10^{-5}	1.6	412	37	22.04	0.85	0.41	0.0145	132 n	-3.3	0.0200	Low I_g , Ni gate
1-1535-4	8.30 x 10^{-5}	2.2	640	133	19.33	4.45	0.31	0.032	45 n	-2.2	0.034	Good performance
1-1534-5	7.7 x 10^{-5}	6.4	535	212	22.1	3.5	0.33	0.0654	23 n	-2.12	0.053	Good performance
1-1536-1	4.42 x 10^{-6}	4.02	601	236	16.10	1.97	0.35	0.032	1 m	-2.4	0.0165	Large I_g , Ni/Au gate
1-1536-6	7.7 x 10^{-6}	2.47	628	145	19.3	1.54	0.3	0.0574	1 m	-2.5	0.0263	Large I_g , Ni/Au gate
1-1639-1	6.3 x 10^{-5}	3.77	632	297	22.1	3.44	0.27	0.045	19 n	-1.81	0.0567	Good performance
1-1639-2	7.4 x 10^{-5}	6.43	673	303	23.4	1.67	0.25	0.023	23 n	-1.9	0.064	Good performance
1-1643-1	4.42 x 10^{-5}	4.12	581	163	26.1	2.97	0.22	0.062	47 n	-1.6	0.0665	Good performance
1-1643-2	7.30 x 10^{-5}	7.47	618	239	19.5	1.54	0.21	0.0534	54 n	-1.75	0.0363	Good performance

4.6 Multi-fingered devices

After the fabrication process was developed on two-fingered devices, they were extended to form multi-fingered structures. This section describes the performance of a few important multi-fingered devices, and then summarizes their performance.

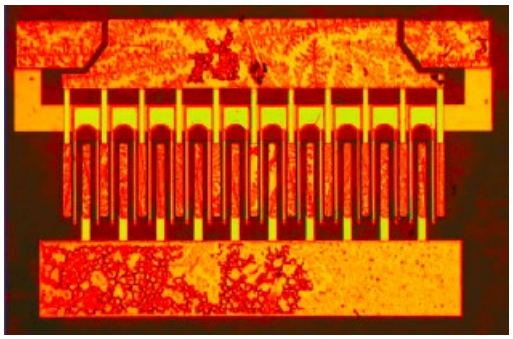
Similar approach to the two-fingered unit cell devices, a design variation was performed on the multi-fingered structures, as seen in previous sections.

Key challenges in the fabrication of multi-fingered devices is to achieve high gate yield, uniform passivation etch, and uniform epitaxial layer growth. Gate yield was an issue as the gate widths for each ranged from 0.5 mm to 40 mm, with the number of fingers ranging from 10 to 40. Issues were also seen in the passivation via etching, which may result in an increase in the turn-on resistance if the etching is not uniform. And lastly, due to non-uniform epitaxial layer, some of the gate-fingers cannot pinch-off, which in turn result in a device failure.

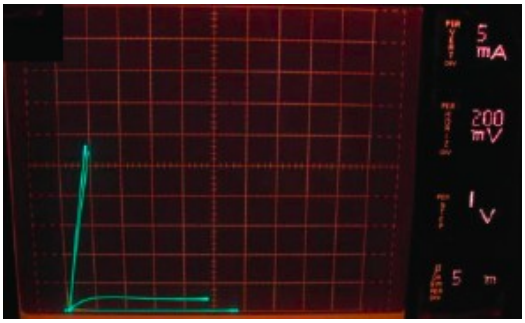
Figure 25 shows the results from a type 2 AlGaN/GaN high-voltage HFET (refer Table 5) device with W_g = 0.2 x 2 mm (4 mm) and L_{gd} = 15 μm. Figure 25(a) shows a microscopic image of the device, and 25(b) and (c) show the I-V (V_{gs} from -4V to 1V) and high voltage off-state IV curves (at V_{gs} = -10V. The threshold voltage for the devices (V_{th}) was estimated to be -2.6 V. The breakdown voltage was over 900 V, as seen in 25(c).

Figure 26 shows the results of a fabricated Type-3 high-voltage HFETs with W_g = 0.5 x 10 mm (5 mm) and L_{gd} = 25 μm. The threshold voltage for the devices (V_{th}) is -2.6 V. The breakdown voltage was 1.4 kV, with a saturated current, I_{dss} = 1.5 Amp.

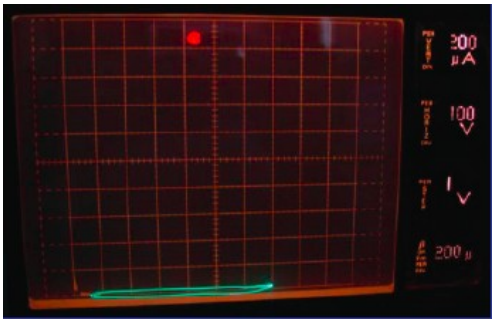
Figures 27, 28, 29, and 30 shows results of fabricated high-voltage AlGaN/GaN HFETs with Types 4, 7, 8, and 9 desgins respectively. It can be inferred from the plots, the breakdown voltage for all devices was larger than 900 V. All these devices exhibited low turn-on resistance (less than 30 18.5 mΩ-cm^2), low gate leakage (¡200



(a)



(b)



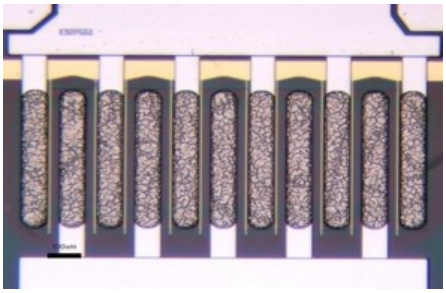
(c)

Figure 25: Multi-fingered devices (Type 2) characteristics (wafer ID: 1-1427-1). Device dimensions: W_g = 4 mm, L_{gd} = 15 μm, $L_g = L_{gs}$ = 3 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 8.9 mΩ-cm^2, and (c) shows BV_{ds}>900 V at V_{gs} = -8V plot.

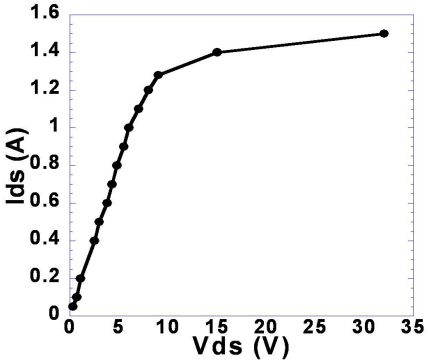
nA at V_{ds} = -200 V), and high breakdown voltage of 800 V.

Figure 31 highlights results obtained from a fabricated lateral Schottky barrier diode with W_g = 5 mm. The breakdown voltage was over 700 V and the turn-on voltage (V_f) is 1.3 V, as seen in Figure 31(c).

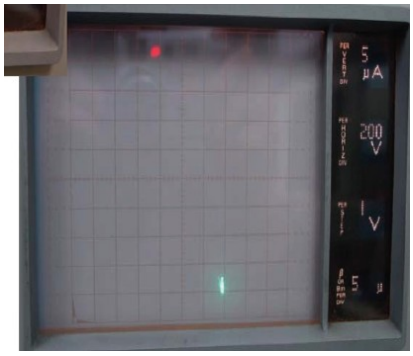
Table 16 gives a summary of the high-voltage performance of all multi-fingered devices (ranging from W_g = 2.4 mm upto W_g = 5 mm). Most devices observed high breakdown voltage characteristics. For device type 1, there was a design error, where the gate and source was shorted, and hence the poor performance. For all other device types, the designs were effective and exhibited excellent high power characteristics. Device Type 3 with W_g = 5 mm was the champion device design, since it had a high BV_{ds} of 1.4 kV and low $R_{ds(ON)}A$ of 29 mΩ-cm^2. The multi-fingered devices formed



(a)



(b)



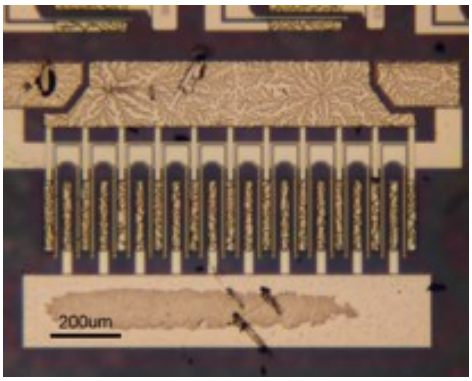
(c)

Figure 26: Multi-fingered devices (Type 3) characteristics (wafer ID: 1-1427-1). Device dimensions: W_g = 5 mm, L_{gd} = 25 μm, $L_g = L_{gs}$ = 3 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 29 mΩ-cm^2 plot, and (c) shows BV_{ds} = 1.4 kV at V_{gs} = -8V plot.

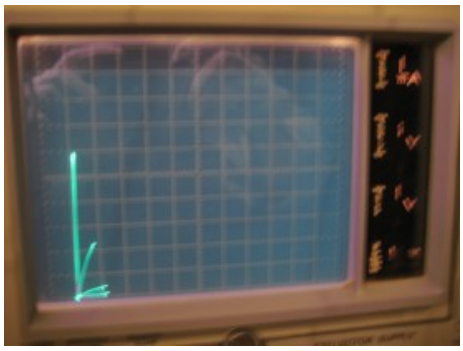
the basis for the design of the large area device. It was seen that L_g of 3 μm and W_g of 500 μm gave the highest yield for gate, and was selected for the device with high-current handling. The L_{gs} of 3 μm gave minimum gate to source resistance in this set of device design and was used for the design of the large area device.

4.7 Working toward 10-Amp Power AlGaN/GaN HFET Transistors

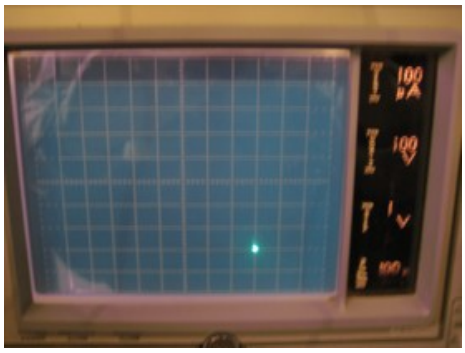
Once the design and fabrication of multi-fingered devices was characterized and optimized, the devices were extended to form large area device, with a targeted W_g = 40 mm. The primary purpose of fabricating this type of HFET design was to produce over 10-Ampere current, and over 600 V breakdown voltage. As observed from previous device types, L_{gd} of 20 μm, $L_g = L_{gs}$ = 3 μm was considered suitable



(a)



(b)

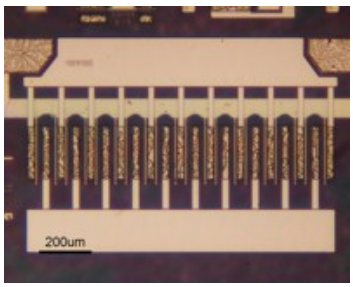


(c)

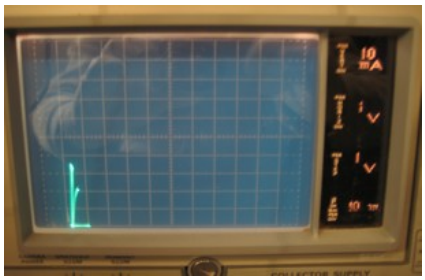
Figure 27: Multi-fingered devices (Type 4) characteristics (wafer ID: 1-1439-6). Device dimensions: W_g = 3 mm, L_{gd} = 15 μm, L_g = 3 μm, L_{gs} = 4 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 18.5 mΩ-cm^2 (breakdown voltage curve courtesy of Dr. Zhu, Alpha and Omega Semiconductors), and (c) shows BV_{ds} = 800 V at V_{gs} = -8V plot.

for high power performance. These devices were characterized on full 2-inch wafers. For each wafer, statistical data was obtained from TLM, metal-sheet resistance, via access resistance, and two-fingered to multi-fingered devices.

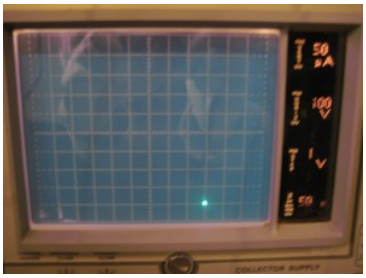
Figure 32 shows the results from a fabricated device on wafer ID: 1-1410-6. Figures 32(a) and 32(b) provide images of the 40 mm device. On every 2-inch wafer, nearly 144 devices were fabricated, and each device property was characterized for good statistical control. Each device has a device area of 2.2 x 2.5 mm^2. As seen in Figure 32(c), the turn-on resistance was as low as 0.8 Ω, and as seen in Figure 32(d), the device exhibited breakdown voltage larger than 600 V, with leakage current less than 1 μA.



(a)



(b)



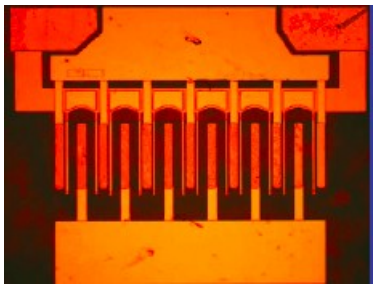
(c)

Figure 28: Multi-fingered devices (Type 7) characteristics (wafer ID: 1-1439-6). Device dimensions: W_g = 4 mm, L_{gd} = 20 μm, $L_g = L_{gs}$ = 3 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 18.5 mΩ-cm^2, and (c) shows BV_{ds} = 1 kV at V_{gs} = -8V plot.

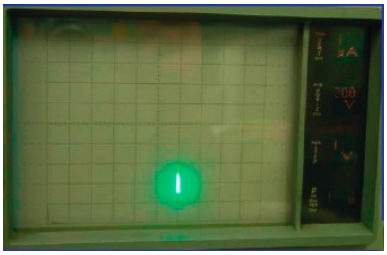
4.8 Challenges and Failure Analysis

After the initial challenge of optimizing the design and layout, fabrication issues such as mesa isolation etch, optimized ohmic temperature anneal, gate metal selection, and passivation etch techniques needed to be tackled. In the previous sections, mesa isolation etch, ohmic and gate metal layers have been discussed.

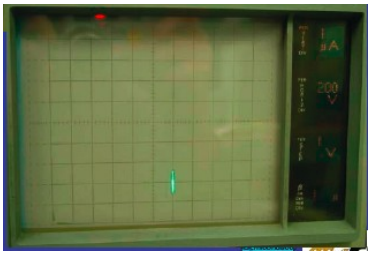
With regards passivation, BCB was used. Initially, a blanket etch was performed on the BCB before a selective etch. This affected the GaN surface, and all devices could not perform above 350 V. However, once the blanket etch step was removed, device performance improved significantly in terms of breakdown voltage. Another major challenge was increasing the yield of the devices on 2-inch wafers. In order to boost the yield, it was important to understand the nature of failures. This section reports some common failure mechanisms observed.



(a)



(b)



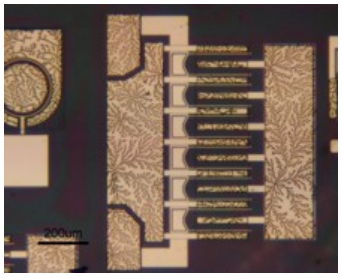
(c)

Figure 29: Multi-fingered devices (Type 8) characteristics (wafer ID: 1-1439-6). Device dimensions: W_g = 2.4 mm, L_{gd} = 25 μm, L_g = 3 μm, L_{gs} = 4 μm. (a) shows the micrscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 15.1 mΩ-cm^2, and (c) shows BV_{ds} = 1.2-1.4 kV at V_{gs} = -8V plot.

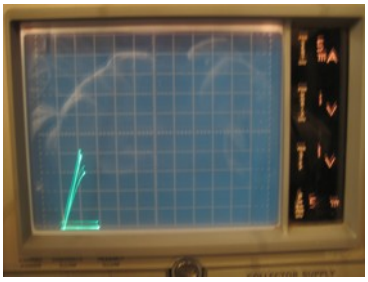
The first and most common type of failure observed was gate-to-drain breakdown (Figure 33), where the breakdown occurred between the gate and the drain. Figure 33(a) shows an image of the failure type, and Figure 33(b) shows the results of the characterization. This failure type mechanism observed when the gate metal blew-up.

The second type of failure observed was gate-to-source shorting (Figure 34). Gate and source demanded critical alignment tolerance. Figure 34(a) shows the microscopic image the the failure, and Figure 34(b) shows the characterization result. This failure mechanism was resolved with good alignment, and a constant source-gate distance of 3 μm across all devices.

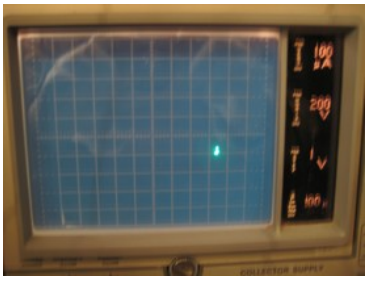
The third type of failure observed was the fabrication of gate fingers (Figure 35). The W_g of the gate was 500 μm and the L_g was 3 μm. There were 80 fingers for each device, and hence fabricating the gate was a challenge. Therefore, a few devices on the 2-inch wafer exhibited poor gate yield. Figures 35(a) and (b) show the microscopic



(a)

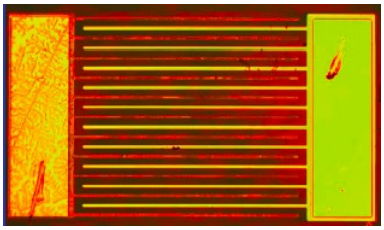


(b)

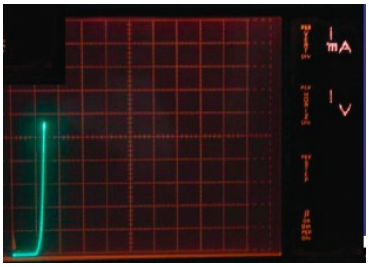


(c)

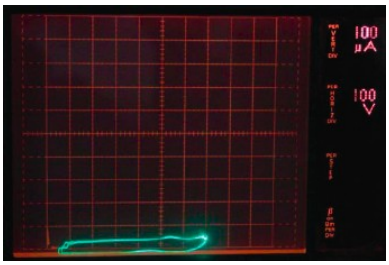
Figure 30: Multi-fingered devices (Type 9) characteristics (wafer ID: 1-1439-6). Device dimensions: W_g = 2.4 mm, L_{gd} = 25 μm, $L_g = L_{gs}$ = 4 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 18.5 mΩ-cm^2, and (c) shows BV_{ds} = 1.6 kV at V_{gs} = -8V plot.



(a)



(b)



(c)

Figure 31: Diode device (Type 11) characteristics (wafer ID: 1-1427-1). Device dimensions: W_g = 5 mm, L_{gd} = 5 μm, L_g = 5 μm. (a) shows the microscopic image, (b) shows the I-V curve with turn-on characteristics, $R_{ds(ON)}A$ = 18.5 mΩ-cm^2, V_f = 1.3 kV, and (c) shows BV_{ds} > 700V, I_r = 80 μA at 600 V plot

Table 16: Performance summary of multi-fingered devices.

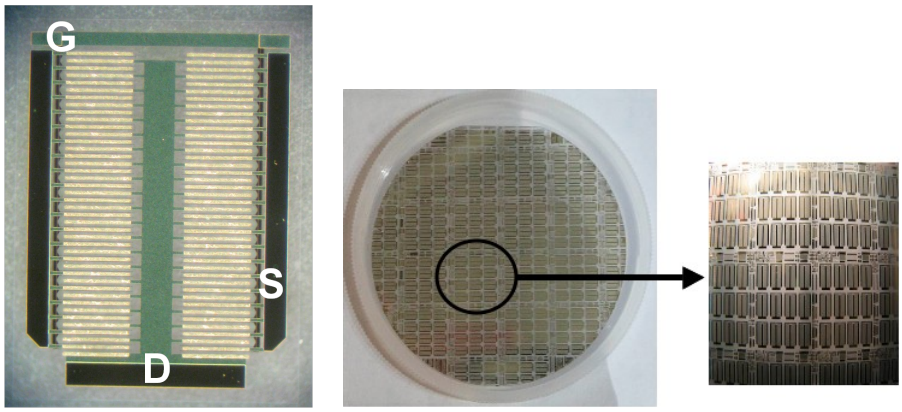
Device no.	**Active Area** (cm^2)	$\boldsymbol{R}_{ds(ON)A}$ (mΩ-cm^2)	$\boldsymbol{L}_{gd}$ (μm)	$\boldsymbol{BV}_{ds}$ (kV)
1	0.00253	N/A	25	0V (Device design issue)
2	0.00215	8.6-12.9	15	>0.8
3	0.00590	29	25	>1.2
4	0.00206	18.5	15	0.7
5	0.00154	11.8	25	>1.2
6	0.00140	25.8	30	>0.8
7	0.00235	13.6	20	>0.7
8	0.00154	15.1	25	>1.2
9	0.00154	14.6	25	>1.4
10	0.00235	15.3	20	>0.8
11	0.00227	227	5	> 0.7

images the the failure type.

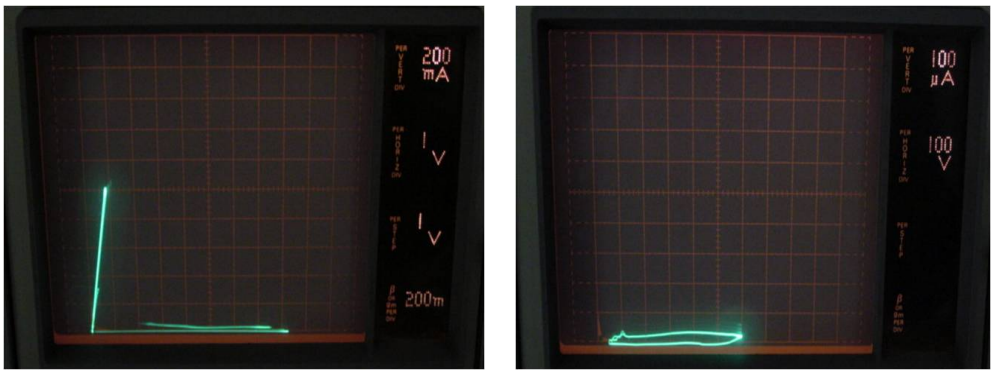
The fourth type of failure observed was BCB-formation (Figure 36). BCB is highly sensitive to O_2, and therefore, even a small amount of O_2 can affect the properties of BCB while curing. For a few wafers, BCB formation issue in terms of uniformity and surface roughness was observed, as seen in Figures 36(a) and (b).

The fifth and types of failure observed were metal contact issue (Figures 37 and 38). It was observed that if the BCB was not etched effectively, the metal pads formed a poor contact with the gate, source or drain. The characterization results showed very poor (infinite) resistance (please refer Figure 37(b)).

The seventh type of failure observed was buffer leakage (Figure 39). Pad to pad probing showed high leakage characteristics (Figure 39(b)). This was commonly seen on wafers with AlN binary barrier.

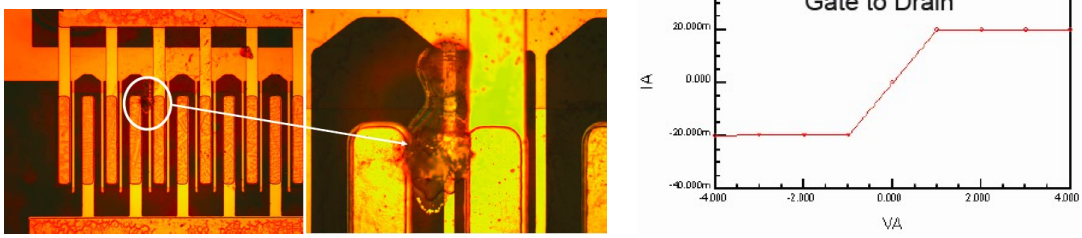


(a) (b)



(c) (d)

Figure 32: Multi-fingered large area device: $W_g = 40$ mm, $L_{gd} = 20$ mm, $L_g = L_{gs} = 3$ μm. Wafer ID = 1-1410-6. Breakdown voltage curve courtesy of Dr. Zhu, Alpha and Omega Semiconductors. (a) shows the device picture with $W_g = 40$ mm, (b) shows a picture of the full 2-inch wafer, (c) shows I-V curve with $R_{ds(ON)A} = 0.8$ Ω, and (d) shows $BV_{ds} > 600$ V plot.

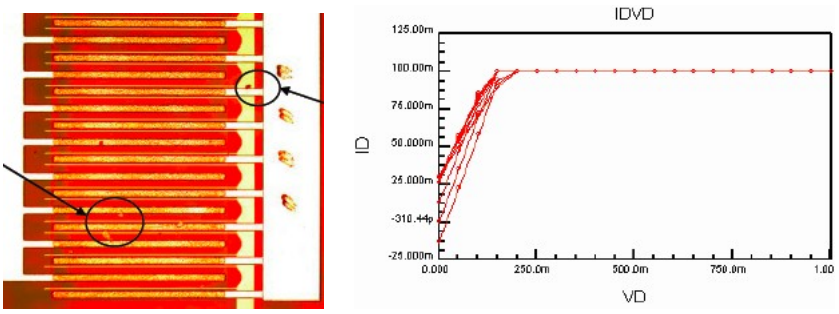


(a) (b)

Figure 33: Gate to drain breakdown: The failure occurred at the edge of the gate bus. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.

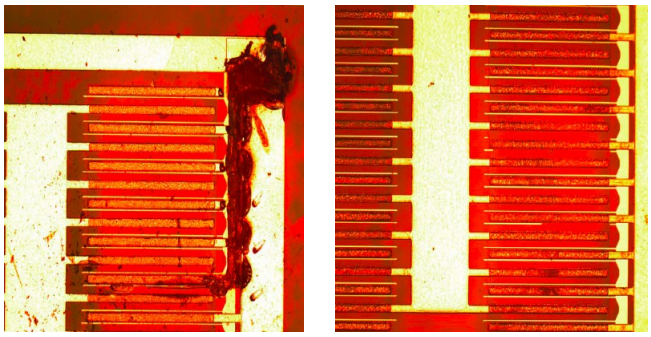
4.9 Summary of Achievements

This work showed the successful fabrication of high power HFETs. Various high-power performance parameters were measured and reported. After two-fingered devices were successfully fabricated and the process was optimized, multi-fingered devices were fabricated. Once the multi-fingered devices were fabricated, they were



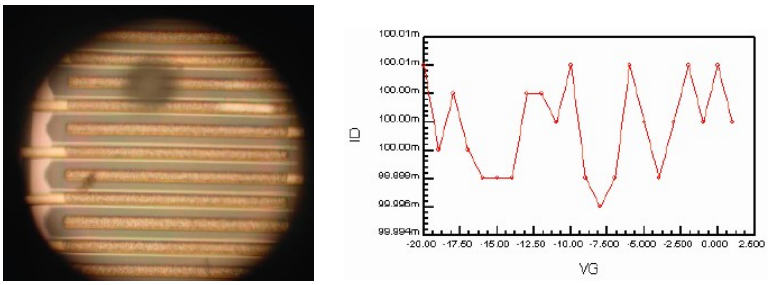
(a) (b)

Figure 34: Gate to source short failure type. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.



(a) (b)

Figure 35: Gate formation issue observed. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.



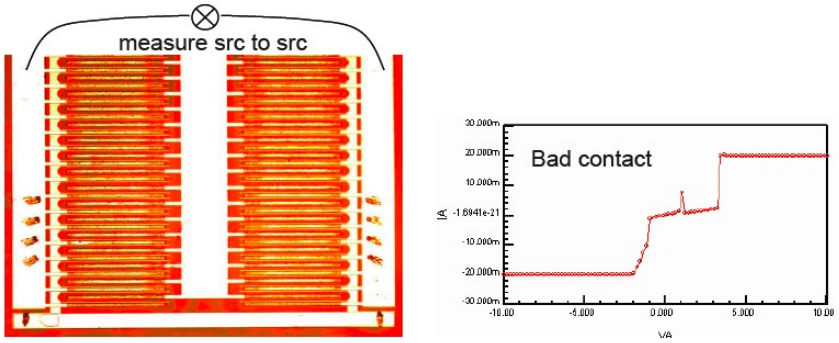
(a) (b)

Figure 36: BCB formation issue observed. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.

extended to form large area power devices. The fabrication techniques were developed for high power AlGaN/GaN HFETs. Unit cell structures demonstrated a performance of over 800 V, with low turn-on resistance. The multi-fingered structures also demonstrated 800V to 1400 V of breakdown, depending on the L_{gd} value.

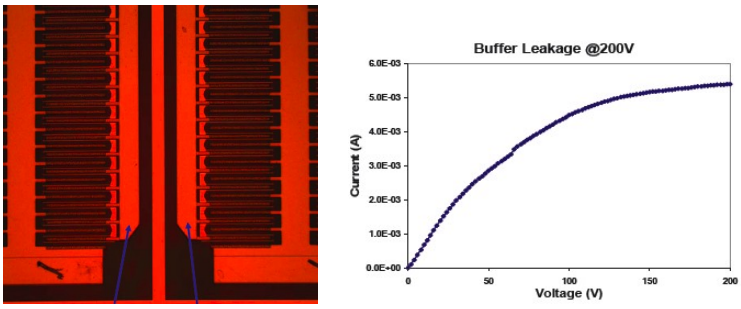
(a) (b)

Figure 37: Metal pad to gate bus contact issue. PCM shows infinite resistance for bad contact. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.



(a) (b)

Figure 38: Metal pad to source contact issue. PCM shows infinite resistance for bad contact. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.

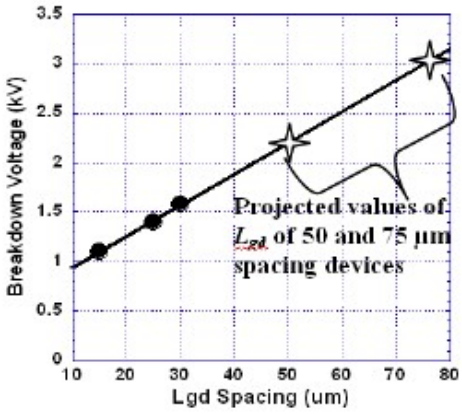


(a) (b)

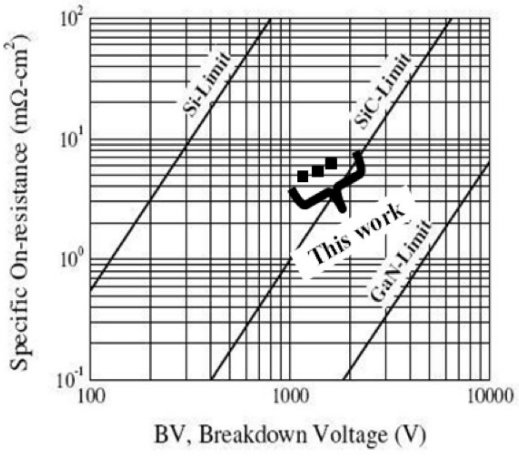
Figure 39: Buffer leakage problem - epi issue. Pad to pad probing shows high leakage current. Courtesy of Dr. Zhu, Alpha and Omega Semiconductors.

And finally, the large area power devices exhibited a breakdown voltage of 600 V. A few major challenges included ICP etching, ohmic resistance, gate metal leakage and passivation etch. These challengesinvestigaed, as reported in the previous sections. Figure 40 shows the competitive position of the wafers fabricated in this work. Fabricated devices show 100X $R_{ds(ON)}A$ compared to Si power devices. The L_{gd} vs. BV_{ds}

variations followed a linear dependence, as shown in Figure 40 (a).



(a)



(b)

Figure 40: High-voltage HFETs fabricated for this thesis. (a) shows a graph indicating the linear dependance of L_{gd} versus breakdown voltage, and (b) shows the $R_{ds(ON)A}$ versus breakdown voltage comparison which indicates significant improvement compared to Si power devices.

CHAPTER V

CONCLUSION

This thesis focused on the design and fabrication of high voltage HFETs on sapphire substrates. The work was divided into three major parts of device fabrication development. First, two-fingered unit cell structures were designed and fabricated. Various design parameters such as L_g, L_{gd}, L_{gs}, and W_g were investigated. These unit cell structures were then fabricated, and their performance was evaluated. Once the fabrication process was developed, the next step was to extend these two-fingered unit celled devices to multi-fingered devices. As discussed in the *Results and Discussion* sections, there were several variations in the design parameters with W_g ranging from 100 μm to 5 mm. It is important to optimize the fabrication process, in order to get good control for developing the gate fingers. Challenges were faced in optimizing the ohmic metal stack, gate metal and BCB passivation etch. For ohmic metal, a combination of Ti/Al/Ti/Au was studied, and for the gate metal, Ni-only metal stack was used. The BCB passivation etch was developed using Cl_2 and Ar. Finally, this work also attempted to extend these multi-fingered structures to large area devices, up to $W_g = 40$ mm. The fabrication processing was done on full 2-inch wafers, and preliminary results have been obtained that has great potential for futher manufacturability.

There are many key areas where the performance of the devices can be significantly improved in the future. The first area is the reduction of turn-on resistance, $R_{ds(ON)A}$. This can be achieved by having lower and more uniform sheet resistance, lower metal contact resistance, and improvement of passivation etch techniques. The second area of improvement is in terms of circuit yield, which can be increased by

better process control. The third area of improvement is working toward of higher breakdown voltage. The large area devices typically exhibited BV_{ds} around 600V to 900 V, and it can be improved to over 1 kV, by reducing surface and gate leakage currents. And finally, various novel structures such as AlN binary barrier and InAlN can be grown for device fabrication to improve the electrical properties of the devices.

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